Prepare for Next Generation USB Technology Testing

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Disclaimer

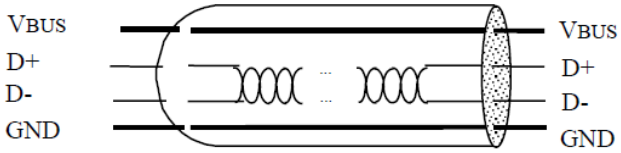
Presentation Disclaimer: The USB 3.1 compliance test requirements are not final therefore all opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of USB-IF or other member companies.

Agenda

- USB updates
- Introduction to USB 3.1 – What's different
- Transmitter Test
- Tx Demonstration
- Receiver Test
- Rx Demonstration
- Summary
- Q&A

Increasing Serial Data Bandwidth

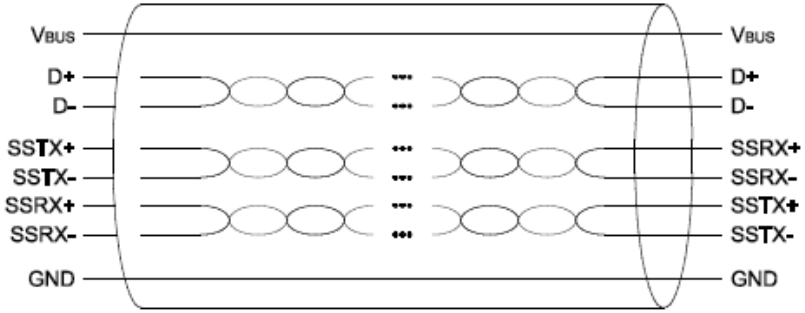
- **USB 2.0, 480 Mb/s** (2000)
  - Shift from slower, wide, parallel buses to narrow, high speed serial bus
  - 40x faster data rate, support for new connectors & charging



High Speed USB Cable

- **USB 3.0, 5 Gb/s** (2008)
  - ~10x faster data rate over 3 meter cable
  - Faster edges, ‘closed eye’ architecture

- **USB 3.1, 5/10 Gb/s** (2013)
  - 2x faster data rate over 1 meter cable
  - ‘Scaled’ SuperSpeed implementation



SuperSpeed USB Cable

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Reference MicroUSB Cable Loss Budget

- Interconnect channel loss (5 Gb/s) can range from ~4dB to ~19dB.
  - Data eye will likely be closed
- Newer mobile products have higher loss
  - Original device budget was 3.5 dB
  - *New* device budget is 7.5 dB
  - Applies for devices with a microUSB connector
- Maintain system loss budget (~19 dB)
  - Reduce cable budget from 7.5 to 3.5 dB
  - Implies shorter 1 meter cable (previously 3m)

7.5 dB

3.5 dB (1m cable)

7.5 dB

Electrical Validation of SuperSpeed USB 10 Gb/s

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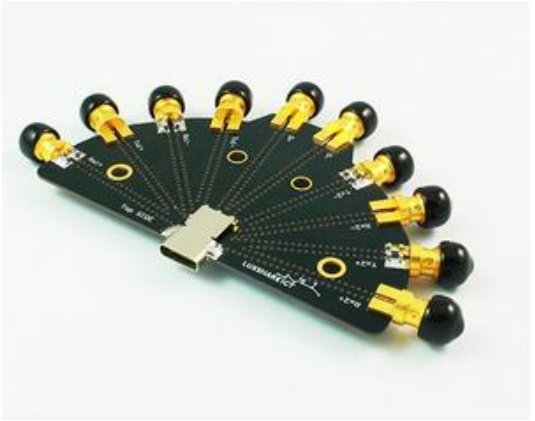
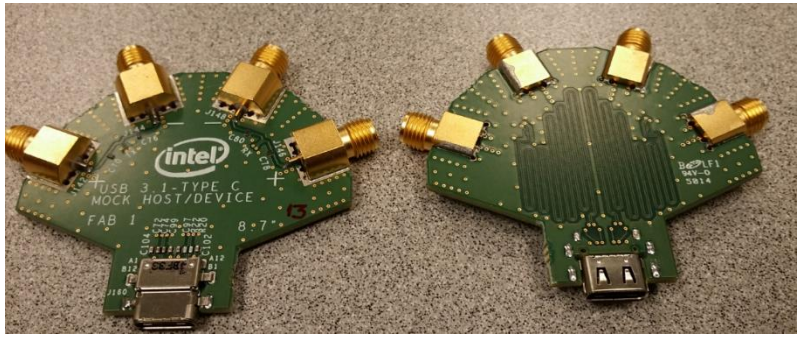
USB 3.1 Fixtures

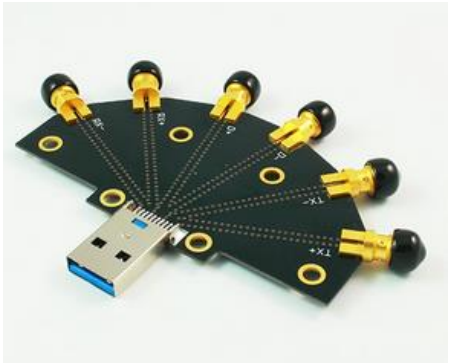
- Official Host/Device (Std/Micro A/B and Type C) fixtures under development
  - Expect orderable Q2 2016 from USBIF
- Luxshare-ICT 3rd party fixtures available
  - USB 3.1 Type A, B, & C
  - Plug, receptacle and calibration fixtures



USB 3.1 C Receptacle Fixture



USB-IF
Sample Type-C Fixtures & Channels



USB 3.1 A Plug Fixture

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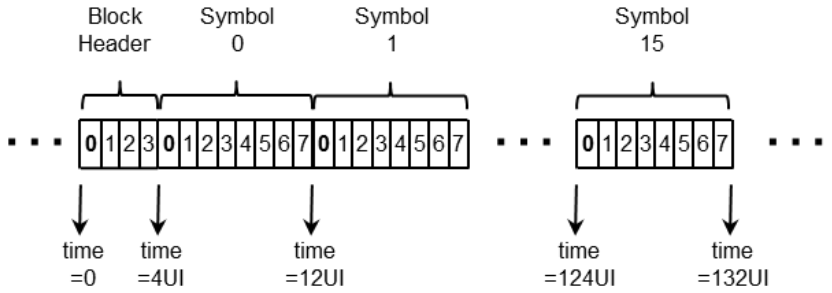
USB 3.1 Comparison

	Gen1	Gen2
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m + Host/Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-20dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	71 ps (0.714 UI)
Backwards Compatibility	Y	Y
Connector	Std A	Improved Std A with insertion detect

128b/132b Encoding and Compliance Patterns

- 4-bit block header (0011 -> control, 1100 -> data)
- 128-bit (16 bytes) non-encoded payload
- Similar to PCI Express but with 4-bit header
  - 1 bit error (self correcting)
  - 2 bit error (detection)
- SKP Ordered Set
  - Clock compensation (+300 to -5300ppm offset)
  - Dynamically inserted/removed Includes
  - LFSR state (good for test equipment)



- Higher order scrambler (X^{23} vs. X^{16})
  - Improves EQ training with long, rich pattern
- Compliance with scrambled data (00h) and Nyquist (Ah)
- Pattern toggle between Gen1 and Gen2

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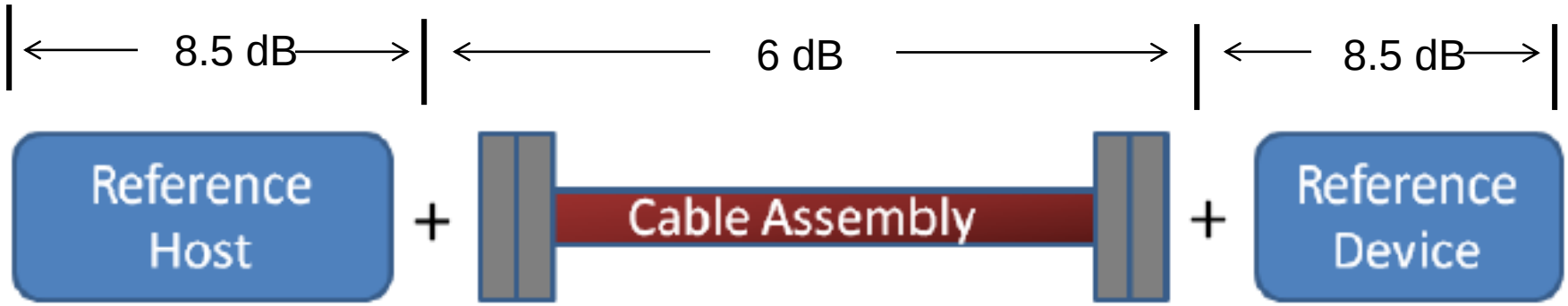
New Channel Budget*

- Target 23 dB @ 5 GHz loss budget (die-to-die)
- Equal channel allocation for host/device
- Tx EQ settings (normative)
  - 2.2 dB Preshoot and -3.1 dB De-emphasis
  - Requires additional compliance patterns for Tx testing
- Host or device loss that exceeds 8.5 dB may required repeater
  - Need end-to-end training -> link aware repeaters



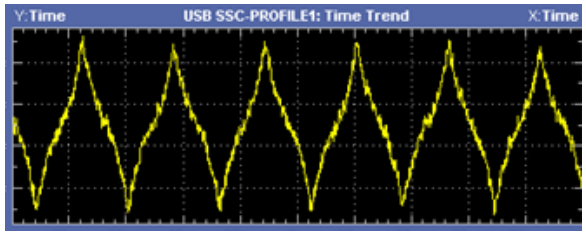
* Items in red indicate new as Aug 2014 release

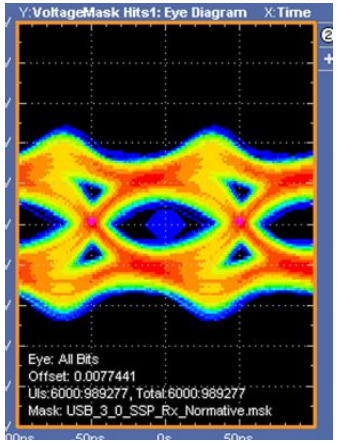
USB 3.1 Transmitter Measurement Overview

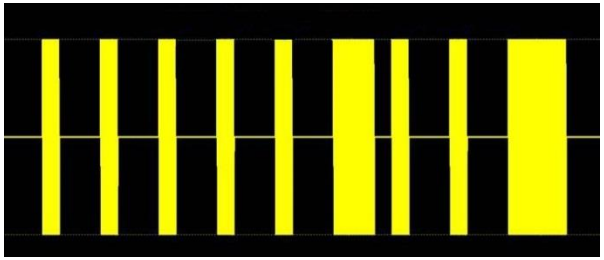
Spec Reference	Parameter
Table 6-16	SSC Modulation Rate SSC Deviation
Table 6-17	Unit Interval including SSC Maximum Slew Rate (5 GT/s) SSC df/dt (10 GT/s)
Table 6-17	Differential p-p Tx Voltage Swing Low-power Differential p-p Tx Voltage Swing De-emphasized Output Voltage Ratio (5 GT/s)
Table 6-18	Tx Min Pulse Deterministic Min Pulse Transmitter DC Common Mode Voltage Tx AC Common Mode Voltage Active
Table 6-19	Transmitter Eye RJ/DJ/TJ - Dual Dirac at 10–12 BER
Table 6-28	LFPS Common Mode Voltage LFPS Differential Voltage LFPS Rise Time LFPS Fall Time LFPS Duty Cycle LFPS tPeriod LFPS tPeriod-SSP (10 GT/s)
Table 6-29	LFPS tBurst LFPS tRepeat
Table 6-31	LFPS tRepeat-0 (10 GT/s) LFPS tRepeat-1 (10 GT/s)
Table 6-32	LFPS Pulse Width Modulation (10 GT/s) tLFPS-0 (10 GT/s) tLFPS-1 (10 GT/s)

PHY
(CP9)

LFPS







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SuperSpeed Transmitter Compliance Testing

1. Connect DUT to scope via test fixture.
2. Transmit CP10 (clock) & measure 10^6 consecutive UI
   - This step used to measure RJ
3. Repeat with CP9 (scrambled data pattern)
   - Will combine RJ (step 2) with DJ to extrapolate TJ (step5)
4. Post-process the waveforms with the compliance channel, the reference CTLE, & jitter transfer function
   - Channels are S-Parameter-based and are embedded into captured waveform
5. Extrapolate jitter to 10^{-12} BER

Spec	Min	Max	Units
Eye Height	70	1200	mV
Dj @ 10^{-12} BER		0.530	UI
Rj @ 10^{-12} BER		0.184	UI
Tj @ 10^{-12} BER		0.714	UI

USB 3.1 Tx

RECOMMENDED TRANSMITTER SOLUTION

- ≥23 GHz BW, 100 GS/sec preferred
- >10M minimum record length allows capture of 1M UI at 100 GS/sec, no interpolation.
- DPOJET for advanced jitter/eye analysis
- SDLA for channel embedding and cycling through 7 CTLE/1 DFE settings
- TekExpress automation software for USB 3.1 gen1/gen2 physical layer validation

For instrument bandwidth, consider factors such as:

- Edge Rate
- Reflections
- SNR (de-embedding)
- Launch Characteristics

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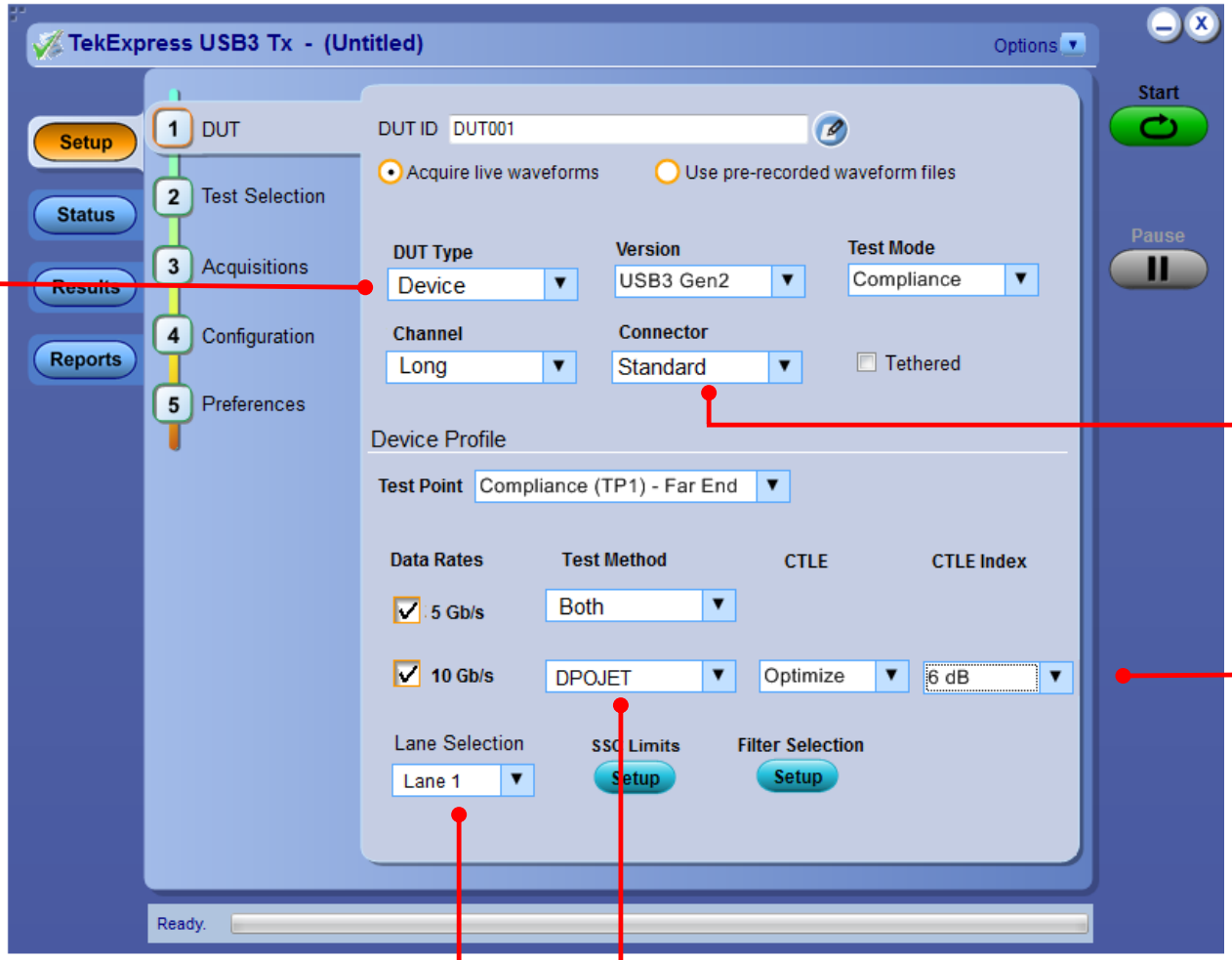
USB Type-C™ Automation



Device, Host or DRD

USB Type-C, Standard, or Micro

Sweep CTLE

Multi-lane automation

Debug (DPOJET) or Compliance (Sigtest)

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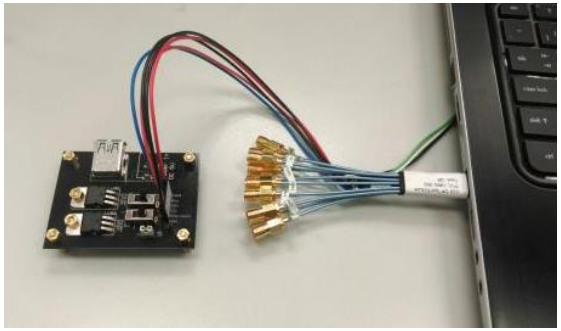
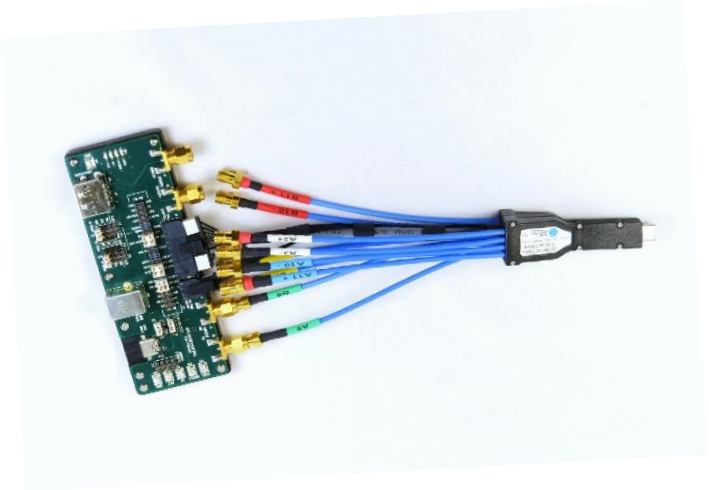
Fixture and Signal Access

USB Type-C™ to USB Std-A adapter (short)

Luxshare-ICT plug fixture with DFP/UFP board



Wilder plug fixture with Alt Mode Control board



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USB, Alt Mode, USB PD Test Setup

DP-AUX

GRL Alt Mode &
USB PD Controller

SBU1/2
(AUX+/-)

CC1/CC2/VCONN/
VBUS/GND

**Wilder Fixture and
Alt Mode Control Board**

DUT

High Speed Signals
(Tx/Rx)

* Automation available through USB control

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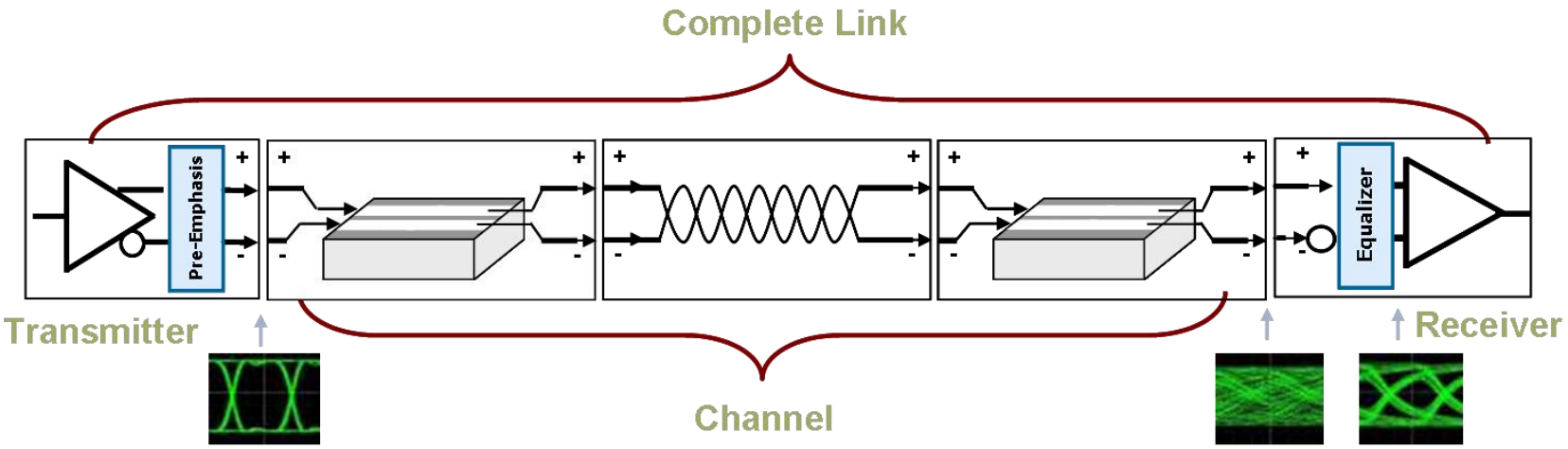
USB 3.1 Receiver Testing Overview

- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions
  - Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
  - Add a specific “recipe” of stresses and de-emphasis
  - Command the DUT into loopback mode (far-end retimed)
  - Return “echoed” data to a BERT
  - Detected errors are inferred to be a result of bad DUT receiver decisions



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JTOL Template Comparison

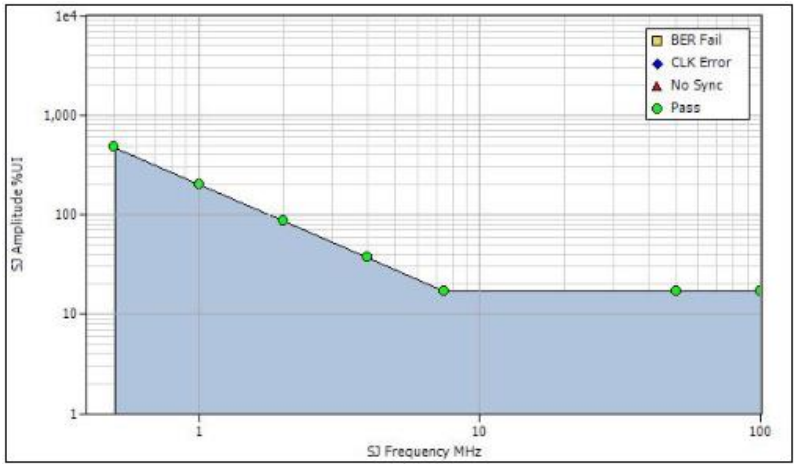
Symbol	Parameter	Gen 1	Gen 2	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.01308	UI rms	1
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	0.184	UI p-p	1,4
J_{Pj_500kHz}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	0.8	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	Pre=2.7 Post= -3.3	dB	1

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-18.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test, though it is not shown in Figure 6-1
5. The JTOL specs for Gen 2 comprehend jitter peaking with re-timers in the system and has a 25 dB/decade slope.

Receiver Tolerance Test Overview

- Seven Test Points
- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- Preshoot/De-emphasis enabled
- Stress verified by TJ/Eye Height
- Each SJ term in the table below is tested one at a time after the device is in loopback mode



MHZ	Test	Template	Bits	Errors	BER	Status	Margin
0.50	476.00%	476.00%	3.00e010	0	0.00e000	Passed	0.00%
1.00	203.00%	203.00%	3.00e010	0	0.00e000	Passed	0.00%
2.00	87.00%	87.00%	3.00e010	0	0.00e000	Passed	0.00%
4.00	37.00%	37.00%	3.00e010	0	0.00e000	Passed	0.00%
7.50	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
50.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
100.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%

Frequency	SJ	RJ
500kHz	476ps	1.308ps RMS
1MHz	203ps	1.308ps RMS
2MHz	87ps	1.308ps RMS
4MHz	37ps	1.308ps RMS
7.5MHz	17ps	1.308ps RMS
50MHz	17ps	1.308ps RMS
100MHz	17ps	1.308ps RMS

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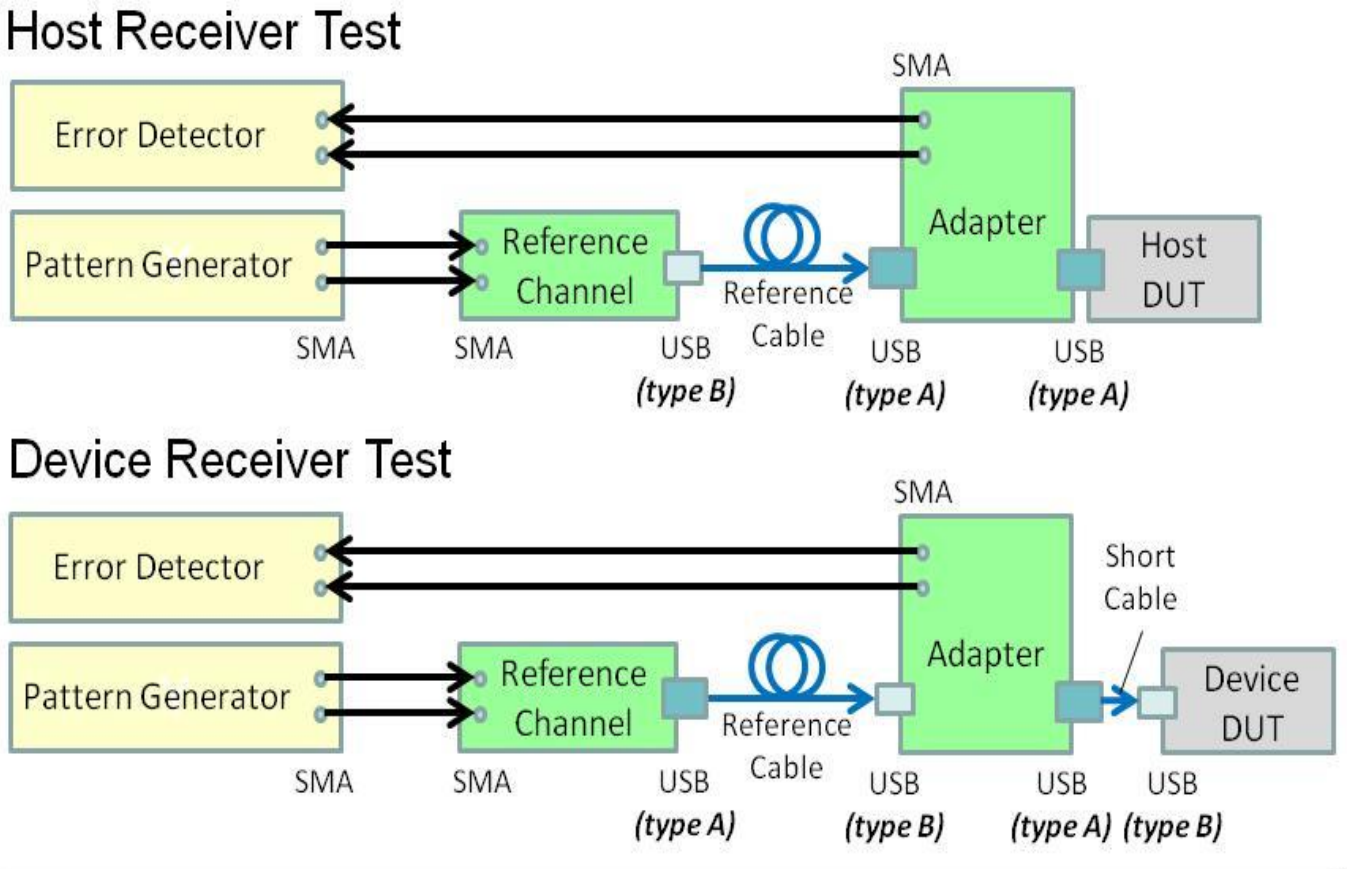
Generic RX Test Configuration



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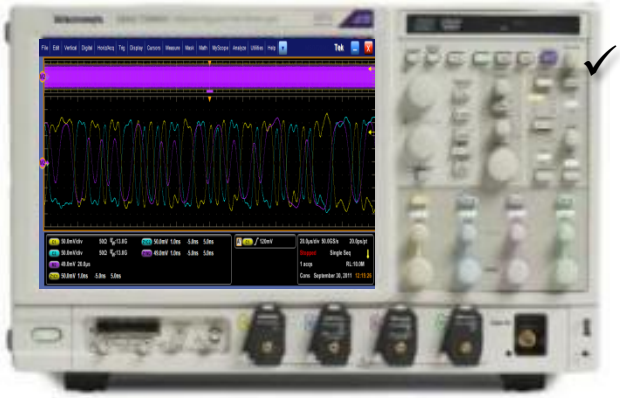
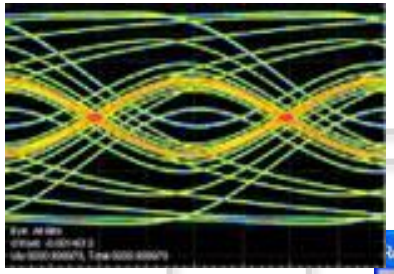
Stress Recipe - Calibration

Long waveform **capture by Real Time Scope**



Tx Eq



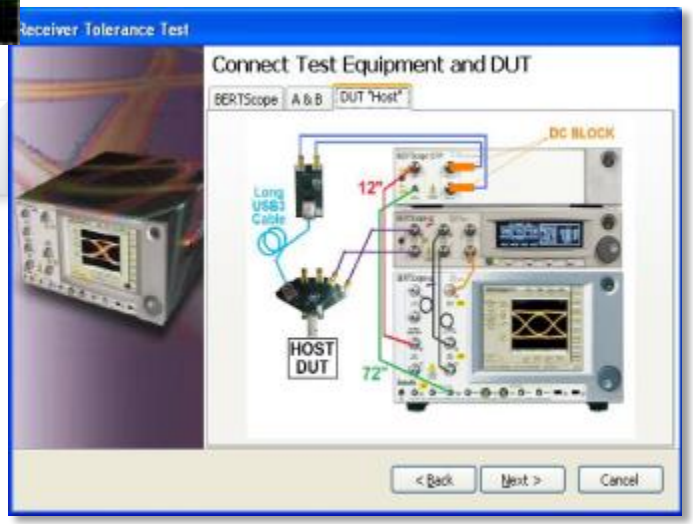
Channel

Test Equipment

SigTest Post-processing

RJ Source

SJ Source



Mature standard with **fully automated** solutions for stress calibration and **good correlation**

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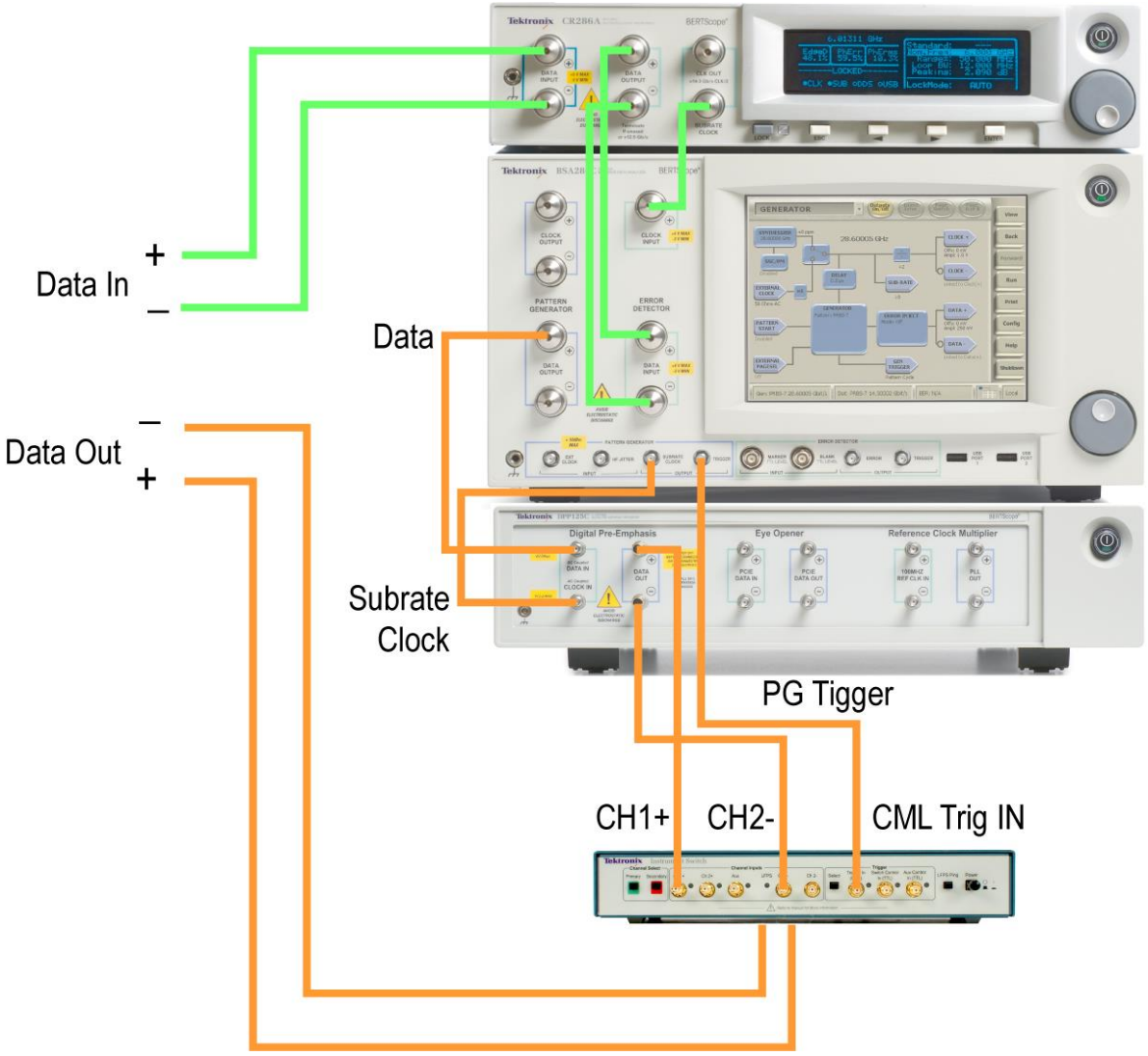
BERTScope USB 3.1 solution



- CR125A Clock Recovery
- BSA125C BERTScope with USB3 Automation software*
- DPP125C De-Emphasis Processor
- USB Switch*
  - Creates the low-frequency periodic signaling (LFPS) required to initiate Loopback-mode

*** Requires updates**

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Summary

- Higher performance with SuperSpeed USB 10 Gb/s
- USB 3.1 adds additional challenges beyond legacy requirements (backwards compatibility)
- Tektronix extensive PHY validation tools for early designs
  - New USBSSP automation for Tx validation
  - BERTScope USB library with JTOL templates
  - Test procedures documented in Methods of Implementation (MOI)

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