70th Anniversary

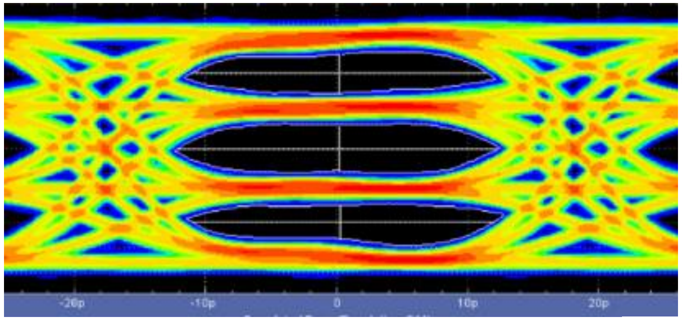
展望太克 榮耀70

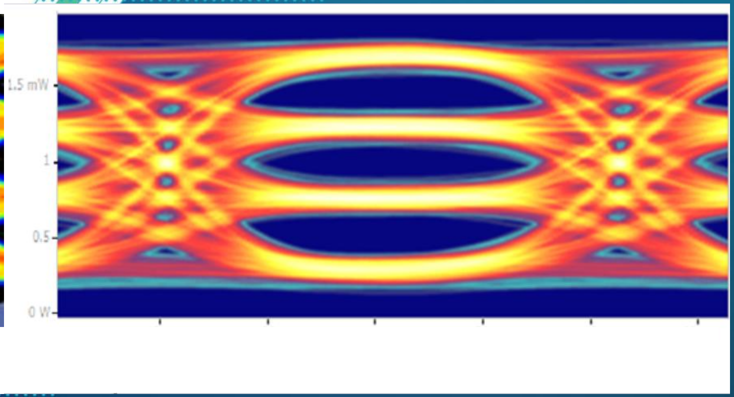
2016太克科技

春季創新論壇

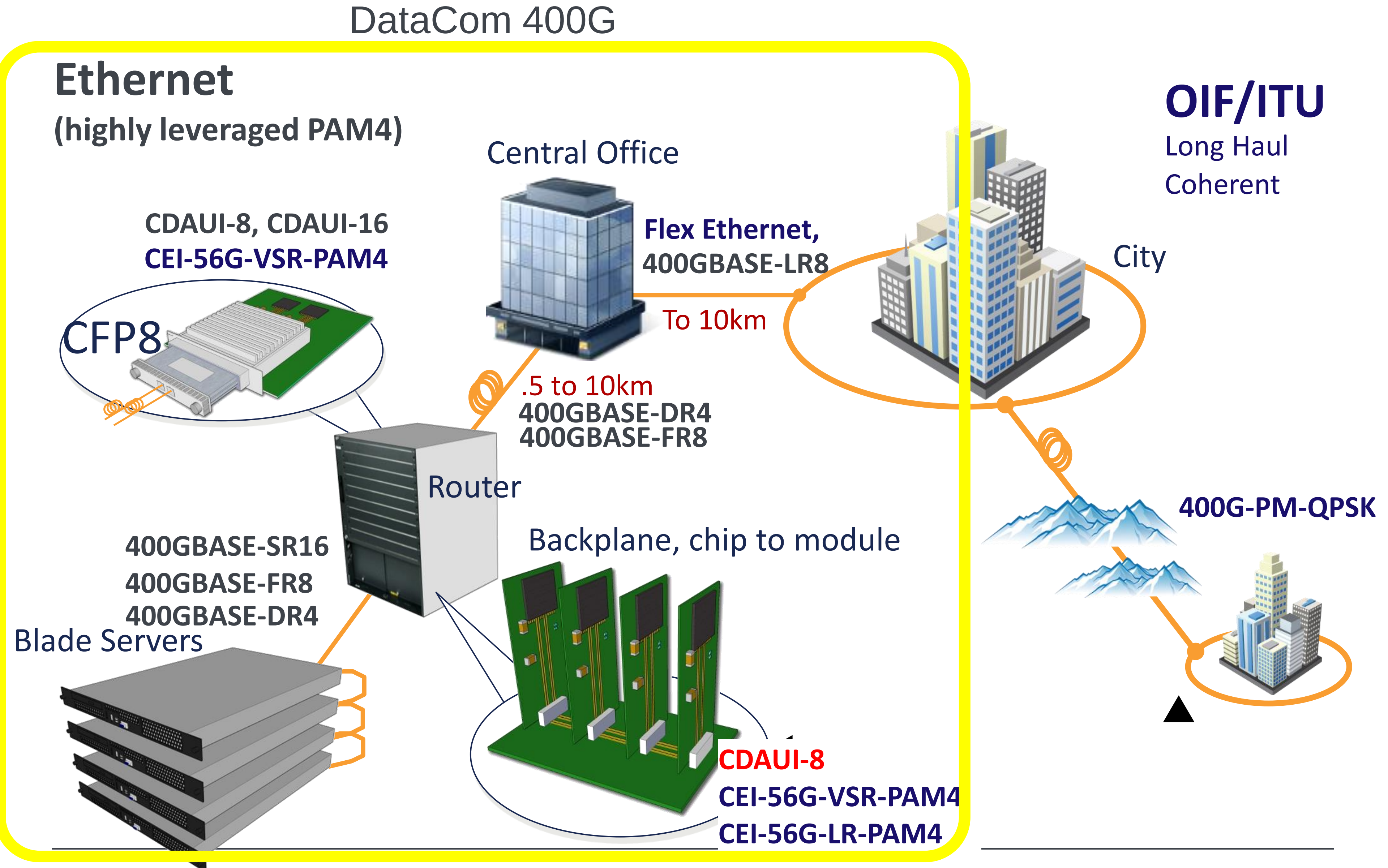
Tektronix®

DataCom: Practical PAM4 Test Methods for Electrical CDAUI8/VSR-PAM4, Optical 400G-BASE LR8/FR8/DR4





400G Ecosystem (shown for comparison)



The Top-to-Bottom *100G* Standards

(Main actors only, not a comprehensive table)

Distance	Standard	Modulation/signaling	e.g.
X,000 km…40 km	OIF, OTN, ITU	Complex optical	DP-QPSK
10, 40 km	Ethernet	NRZ SM	100GBASE-ER4/LR4
2 km	*MSA "CLR4"*	NRZ SM	100G-CLR4
500 m	*MSA "PSM4"*	NRZ SM	100G PSM4
100 m	Ethernet	NRZ MM	100GBASE-SR4
~100 m	Infiniband (IB)	NRZ over active cable; or interconnect	"CAUI-4" going
10 m	Ethernet, IB	NRZ on passive Cu cable	100GBASE-CR4
Backplane < 1m	Ethernet, OIF CEI	NRZ	100GBASE-KR4, CEI LR
		PAM4	100GBASE-KP4
Interconnect module to chip, chip to chip	OIF CEI, Ethernet	NRZ	VSR CAUI-4

100G across the stack

The Top-to-Bottom *400G* Standards

(Main actors only, not a comprehensive table)

Distance	Standard	Modulation/signaling	e.g.
X,000 km	OIF, OTN, ITU	Complex optical	DP-QPSK
100M (MMF)	Ethernet	PAM2 at 25 GBd	400GBASE-SR16
10 km	Ethernet	PAM4 at 25 GBd	400GBASE-LR8
2 km	Ethernet	PAM4 at 25 GBd	400GBASE-FR8
500 m	Ethernet	PAM4 at 56 GBd	400GBASE-DR4
Backplane < 1m	OIF CEI	PAM4 at 25 GBd	CEI LR
Interconnect module to chip, chip to chip	Ethernet OIF CEI	NRZ PAM4	CDAUI-16, CAUI-4 CDAUI-8 CEI VSR PAM4

To 400G across the stack

Why PAM4 now?

Recall the Fibre-Channel 2GFc conversation from 2001 "We're moving to 2Gbps… we need to move to PAM4!"

- 1M Backplane (note KP4) is ~-40dB (Megtron/Comercially viable) of loss (at 13GHz) which is just barely supportable at 100G speeds and current receiver technologies. Doubling of NRZ date rate, pushes backplanes into -70dB loss profiles, and is simply untenable by any known receiver transmitter technology today. Higher order levels of modulation are the most effective way forward, by keeping the signaling fundamental in the range from 12-14GHz.

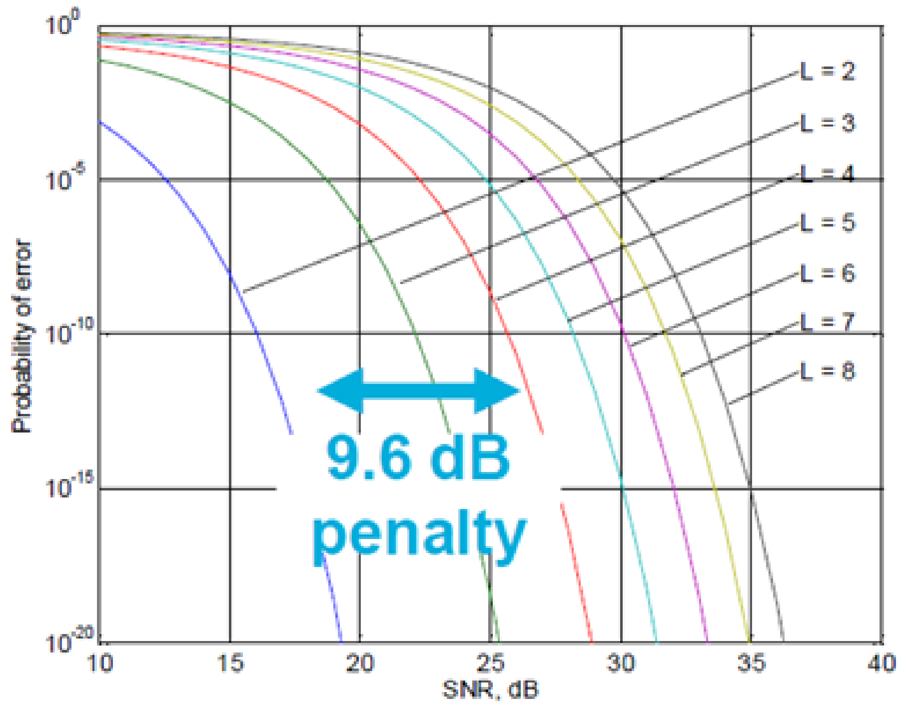
- RX equalization technology has been responsible for making things work up to 25G. Increases in RX dynamic range and sensitivity allow effective multi-threshold sampling of high order modulated signals.

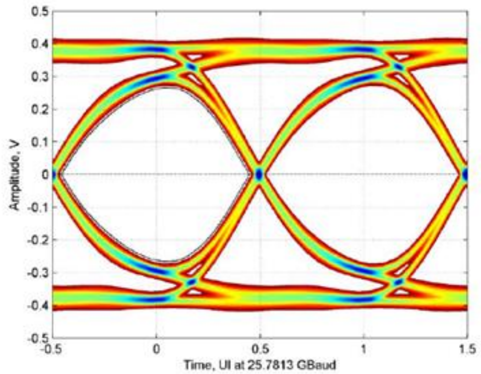
- Optical channels are amenable to 56GBaud, due to the relatively low loss and dispersion. They are going along with PAM4 to maintain the same format and to prevent conversion. The higher order modulation format is not required by the optical domain however.

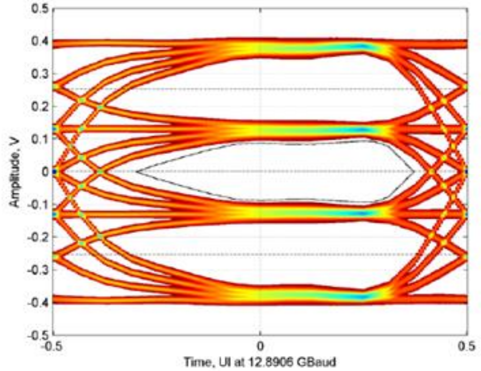
- Commercially viable electrical backplanes and host to module interconnects operating up to 56GBaud are the primary drivers for PAM4.

PAM4 versus NRZ (PAM2) from an SNR viewpoint

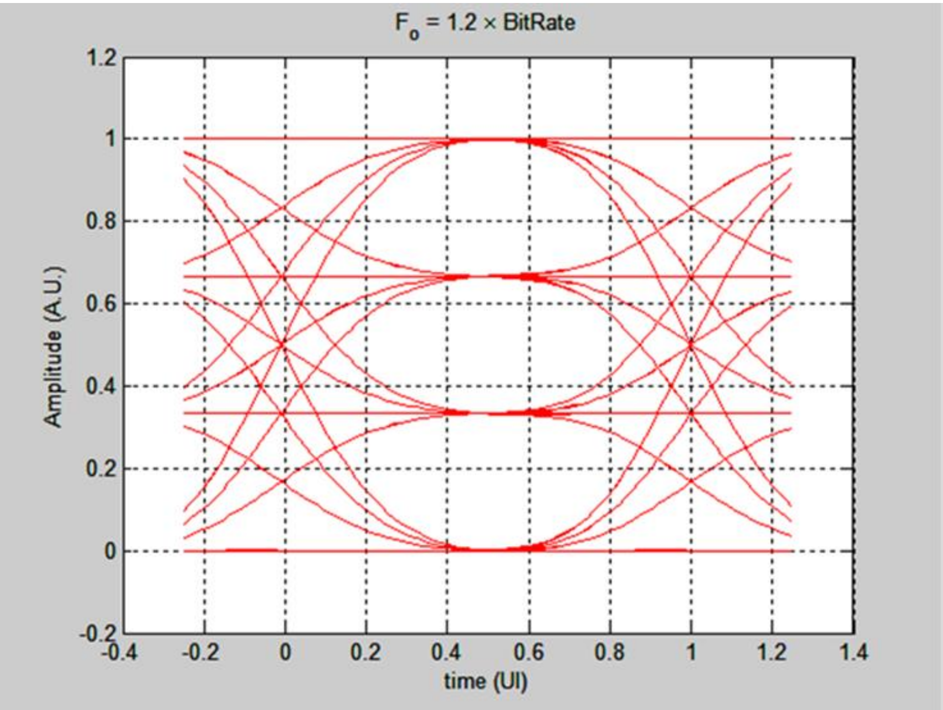
- Channels are ”out of Bandwidth” at 56GBaud.
  - Higher order modulation (PAMn) is one means of combating incredibly high channel losses.
  - Multiple bits/symbols results in a reduced overall symbol rate and fundamental transmission frequency 14GHz rather than 28GHz but comes with a SNR penalty.

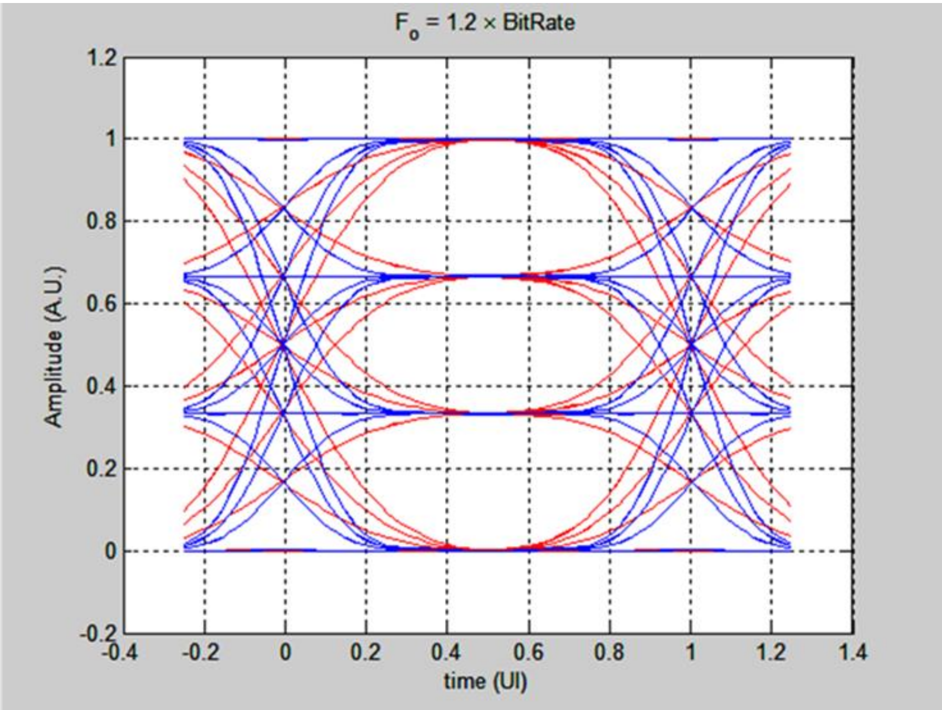






PAM4 (400G) Signal Acquisition Requirements

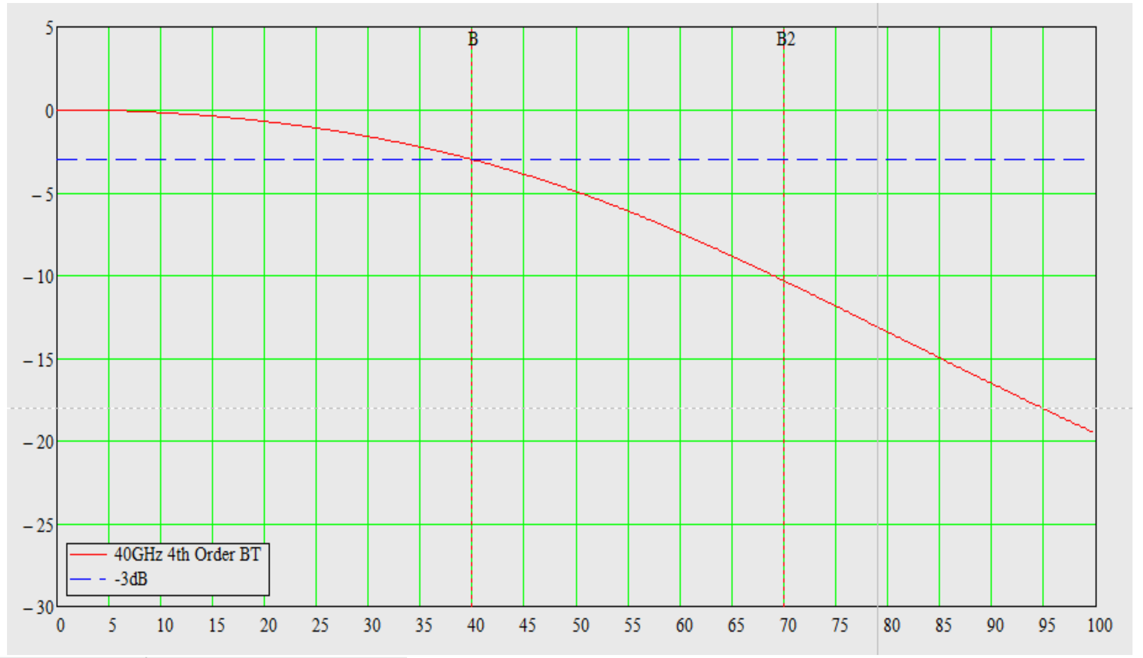


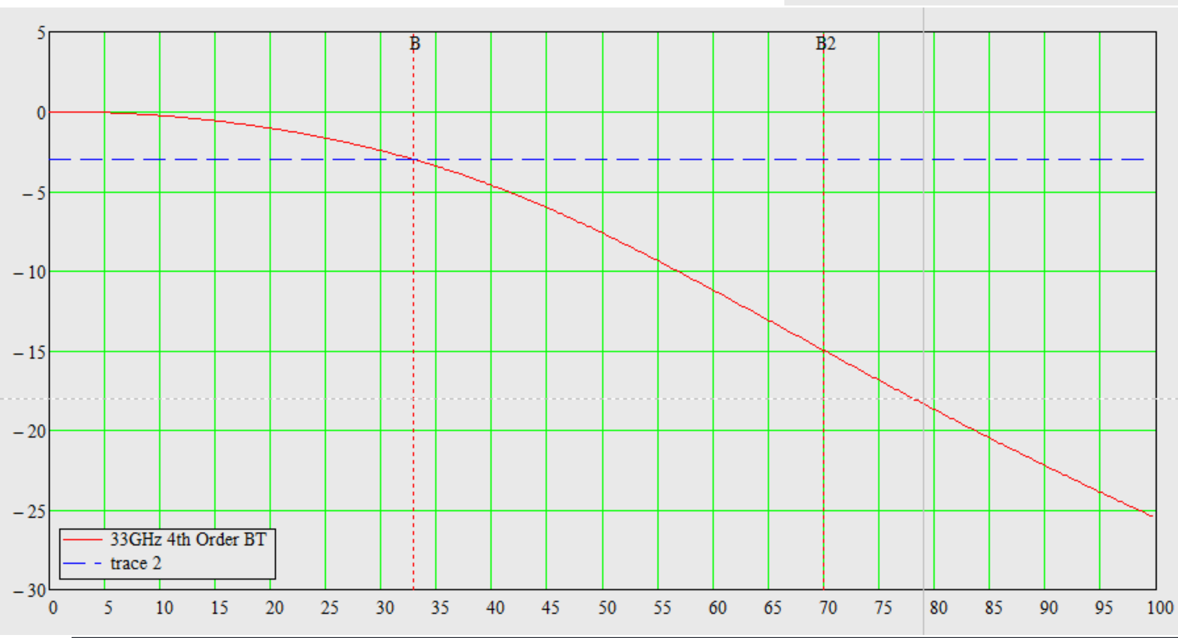


For NRZ (PAM2), the Bessel-Thompson response is traditionally chosen as it has “linear phase” and minimizes instrument induced DDJ. This is not true for a PAM4 signal, where DDJ will be added even for a zero phase filter. This means that a higher BW needs to be used to lower the instrument induced DDJ. The exact amount of extra bandwidth that is needed is still an active area of discussions within the standards group(s). Current discussion seem to be converging in on 120% of the NRZ bandwidth which is typically 1.5x the data rate.

Electrical Bandwidth for PAM4

- Ultimately signal rise time dictates required instrument bandwidth.
- NRZ (PAM2) Electrical BW is commonly called out 1.5x the data rate.
- PAM4 is likely settling on 120% over it's PAM2 needs.





- This ends up being ~1.8x the data rate.
- OIF-CEI (28Gbps NRZ) calls out 40GHz electrical BW (BT response).
- The 28GBaud PAM4 (2X the signal rate) translates to ~48GHz acquisition BW.
- *Remember this is a rule of thumb. Some specs are very precise here.*

State of 400G Optical Communications

Channel	Distance	Lane Rate	Multiplex	Signaling rate	Modulation Format
400GBASE-SR16	100m	16 lane x 25.78Gbps	16 parallel MMF	25.78G Baud	NRZ
400GBASE-DR4	500m	4 lane x 106Gbps	4 parallel SMF	53.12G Baud	PAM4
400GBASE-FR8	2Km	8 lanes x 53.12Gbps	1 SMF 8 λ WDM	26.56G Baud	PAM4
400GBASE-LR8	10Km	8 lanes x 53.12Gbps	1 SMF 8 λ WDM	26.56G Baud	PAM4

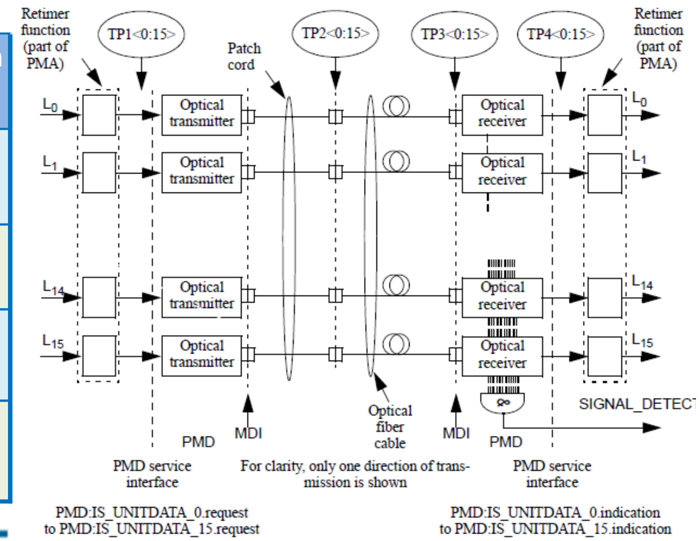
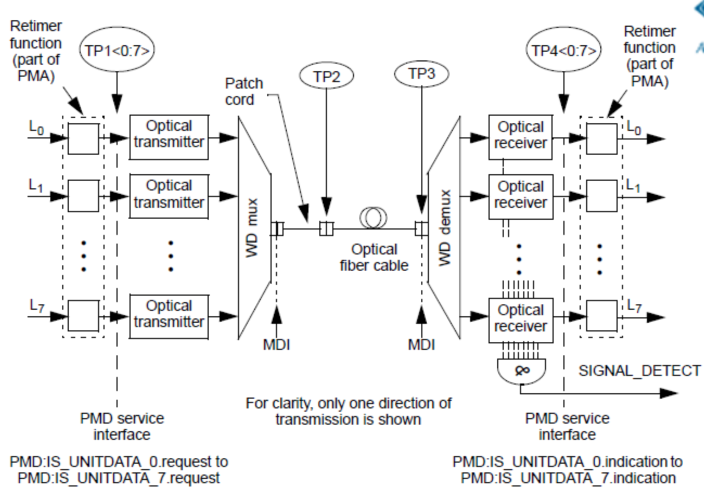


Figure 121–2—Block diagram for 400GBASE-SR16 transmit/receive paths



WD = Wavelength division

NOTE—Specification of the retimer function and the electrical implementation of the PMD service interface is beyond the scope of this standard.

Figure 123–2—Block diagram for 400GBASE-FR8 and 400GBASE-LR8 transmit/receive paths

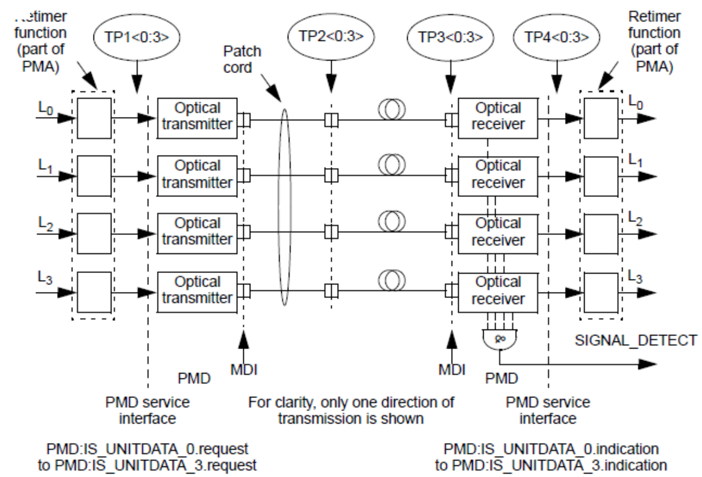


Figure 122–2—Block diagram for 400GBASE-DR4 transmit/receive paths

State of 400G Electrical Communications

Standard	Distance	Lane Rate	Multiplex	Signaling rate	Modulation Format
CEI-56G-XSR-PAM4	50mm	n lane x 56.2 Gbps	1-n lanes electrical	28.1G Baud	PAM4
CEI-56G-VSR-PAM4	150mm	n lane x 56.2 Gbps	1-n lanes electrical	28.1G Baud	PAM4
CEI-56G-MR-PAM4	500mm	n lane x 56.2 Gbps	1-n lanes electrical	28.1G Baud	PAM4
CEI-56G-LR-PAM4	*1000mm*	n lane x 56.2 Gbps	1-n lanes electrical	*28.1G Baud*	*PAM4*
CDAUI-8	250mm	8 lanes x 53.1Gbps	8 lanes electrical	26.56G Baud	PAM4
CDAUI-16	250mm	16 lanes x 26.56Gbps	16 lanes electrical	26.56G Baud	NRZ

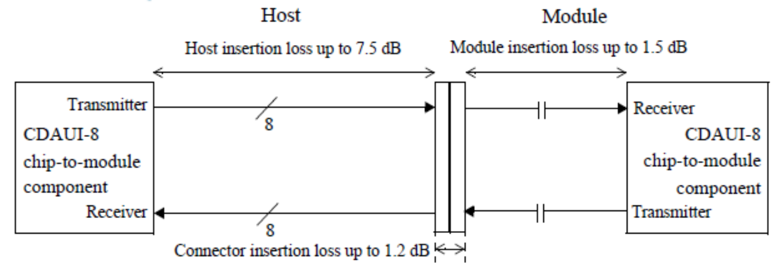


Figure 120E–2—Chip-to-module insertion loss budget at 13.28 GHz

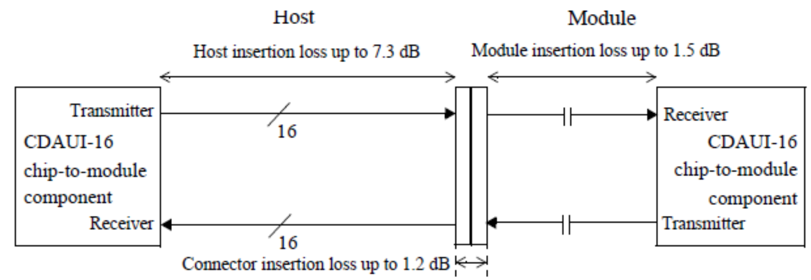


Figure 120C–2—Chip-to-module insertion loss budget at 12.89 GHz

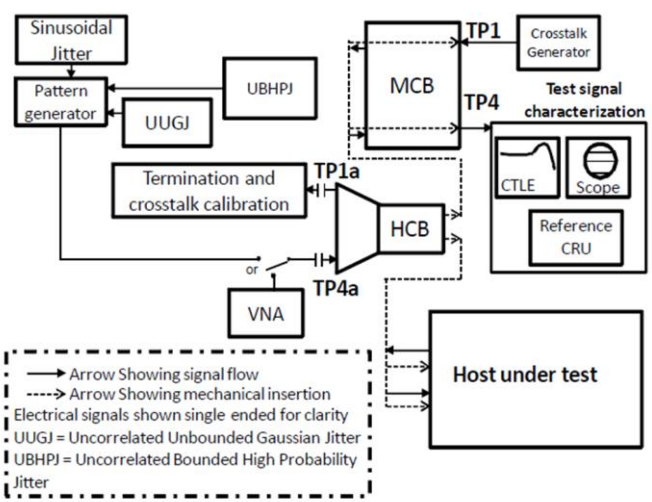
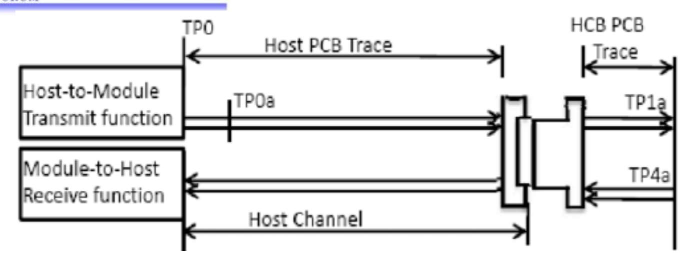


Figure 13-10. Host input test set up



Tektronix 100G/400G Signal Acquisition Systems

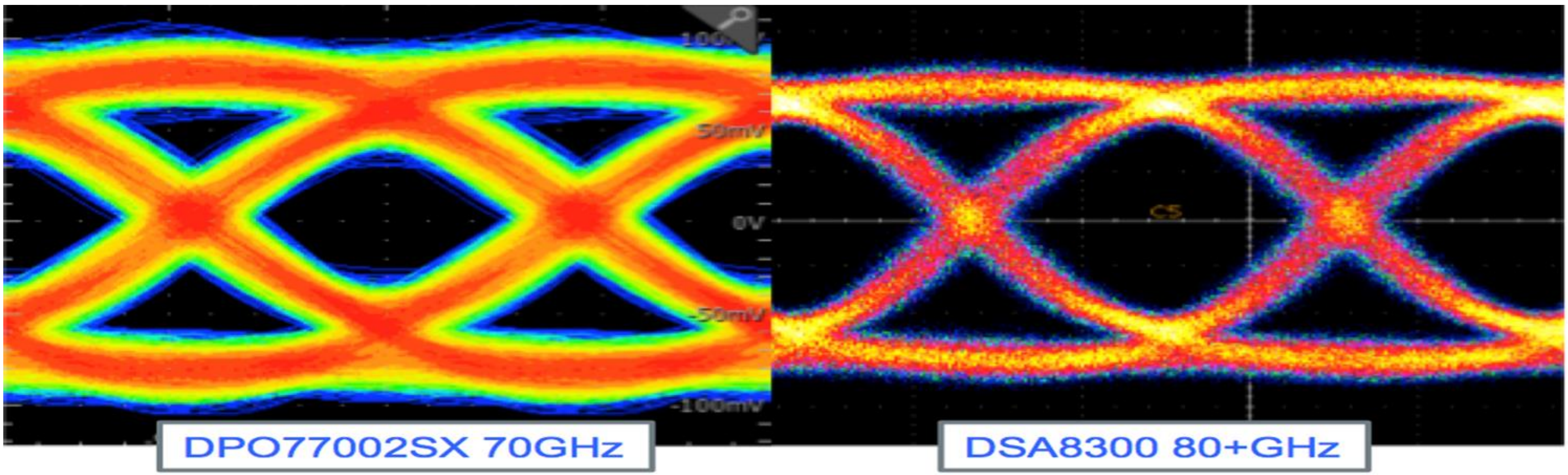
Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis

- **Two world class acquisition systems cover the breadth of any 400G Verification and design needs, with the lowest noise, highest bandwidth in the industry**
  - Real Time (70GHz ATI) single shot acquisition and triggering capabilities are key tools for advanced analysis and debug.
  - Equivalent Time low noise, high sensitivity tools enable the best margin in product and device characterization.

- Real Time
  - 70GHz Analog Bandwidth, 4.3ps rise time (20%-80%)
  - 200GS/s Sample Rate
  - <125fs jitter noise floor
  - ≥25GHz Edge trigger bandwidth
  - Compact 5 ¼” Oscilloscope package
  - No physical clock recovery required (key to 400G)
  - Comprehensive CTLE, DFE, FFE signal processing
  - Lowest noise real time acquisition system
  - Best Electrical solution on the planet

- Equivalent Time
  - 85GHz Optical Bandwidth
  - 70GHz Electrical Bandwidth
  - <100fs jitter noise floor
  - 20nW to .6uW Optical Resolution.
  - Automated test of 80 Industrial Stds.
  - Best Optical solution on the planet

Real Time –vs- Equivalent Time



Tektronix 100G/400G Signal Acquisition Systems

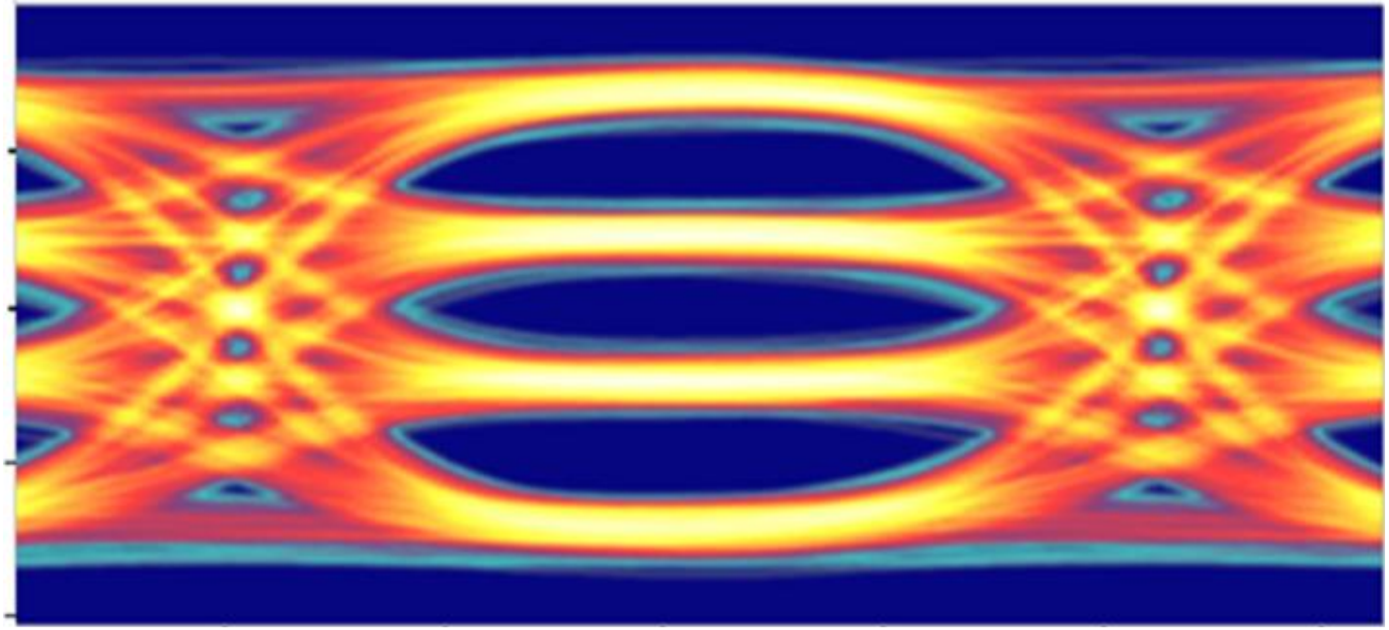
Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis

- **Two world class acquisition systems cover the breadth of any 400G Verification and design needs, with the lowest noise, highest bandwidth in the industry**
  - Real Time (70GHz ATI) single shot acquisition and triggering capabilities are key tools for advanced analysis and debug.
  - Equivalent Time low noise, high sensitivity tools enable the best margin in product and device characterization.

- Real Time
  - 70GHz Analog Bandwidth, 4.3ps rise time (20%-80%)
  - 200GS/s Sample Rate
  - <125fs jitter noise floor
  - ≥25GHz Edge trigger bandwidth
  - Compact 5 ¼" Oscilloscope package
  - No physical clock recovery required (key to 400G)
  - Comprehensive CTLE, DFE, FFE signal processing
  - Lowest noise real time acquisition system
  - Best Electrical solution on the planet

Equivalent Time
- 85GHz Optical Bandwidth
- 70GHz Electrical Bandwidth
- <100fs jitter noise floor
- 20nW to .6uW Optical Resolution.
- Automated test of 80 Industrial Stds.
- Best Optical solution on the planet

80C15 – Multi-Mode/Single-Mode up to 32GBd
80C10C – Single-Mode, 25-32 and 53-56GBd in one



Multi-Mode, Single-Mode: 80C10C vs 80C15

Several key considerations are important in optical analysis.

- Multi-Mode and Single-Mode support are needed to span SR16,LR8, FR8 optical links.
- Noise is THE key spec in optics. The high sensitivity low noise 80C15 is uniquely designed for 28G Baud PAM4 specs (LR8,FR8)
- DR4 specifications require optical BW out to 84 GHz, which is what the 80C10C is designed for.

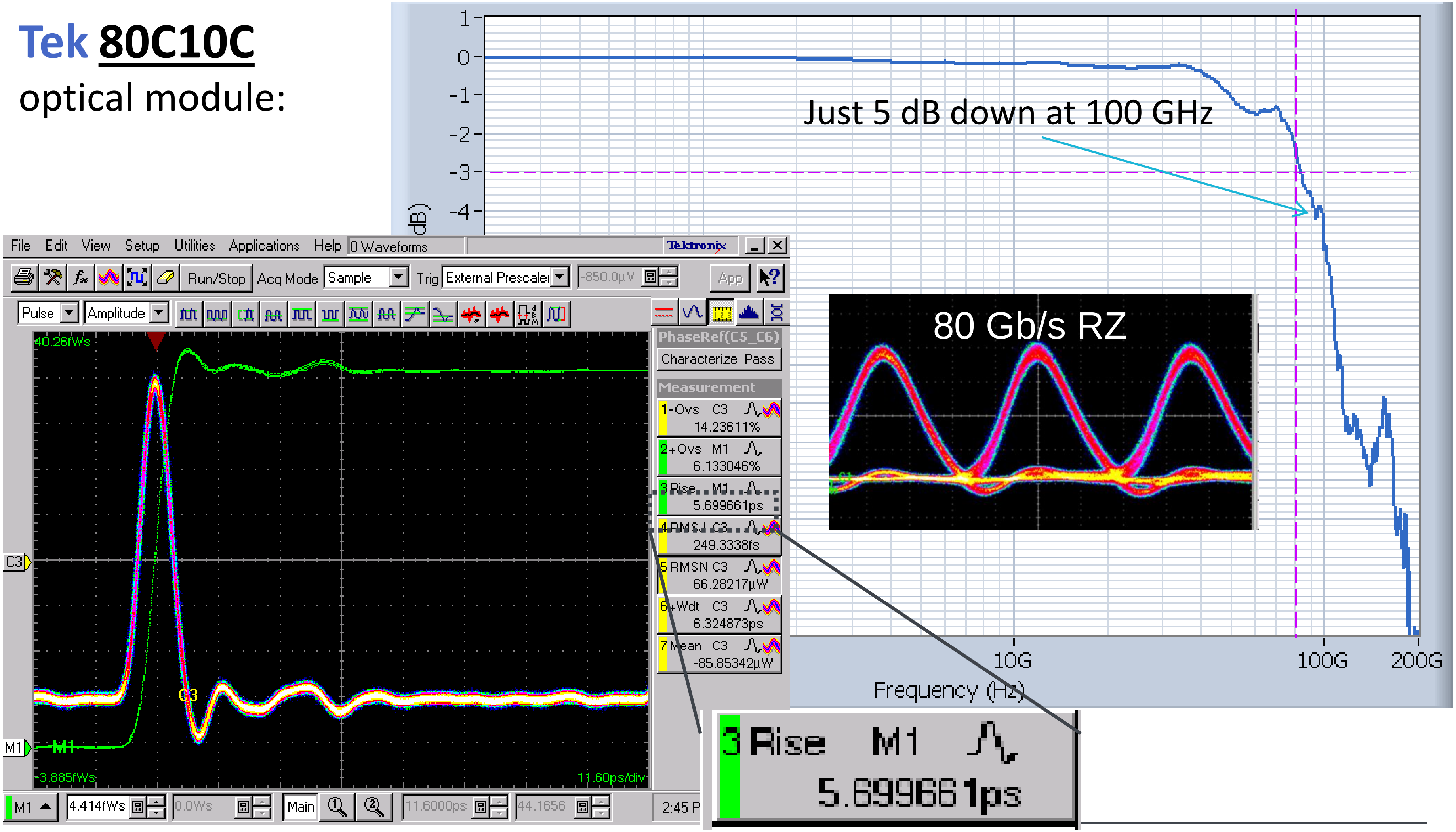
Feature / Specification	80C15	80C10C
Input Fiber Type	SMF + MMF 9, 50, 62.5 µm	SMF 9 µm
Wavelength Range	780nm-1650nm	1290-1620nm
Unfiltered Optical Bandwidth	32+ GHz	80+ GHz
Unfiltered Risetime, typ	14 ps	7 ps opt. F1 6 ps opt. F3
Filter Rates [Gb/s] (not full filter)	TDEC, 26…32	26…**44.5** Gb/s (26G: F1 or F2)
Typ Noise [uW] at 1310 @26Gb/s	10 / 14	16 / NA
26 Gb/s Mask Sensitivity **AOP @ 1310nm**	***-9 dBm***	-6 dBm
Usable Electrical Out ***accessory**	***32 Gb/s***	> 44 Gb/s

Single-mode optical standards

(400Gb/s DR4 specification under development in 802.3bs)

- Current technology satisfies 56 Gb/s as well as current 25 Gb/s

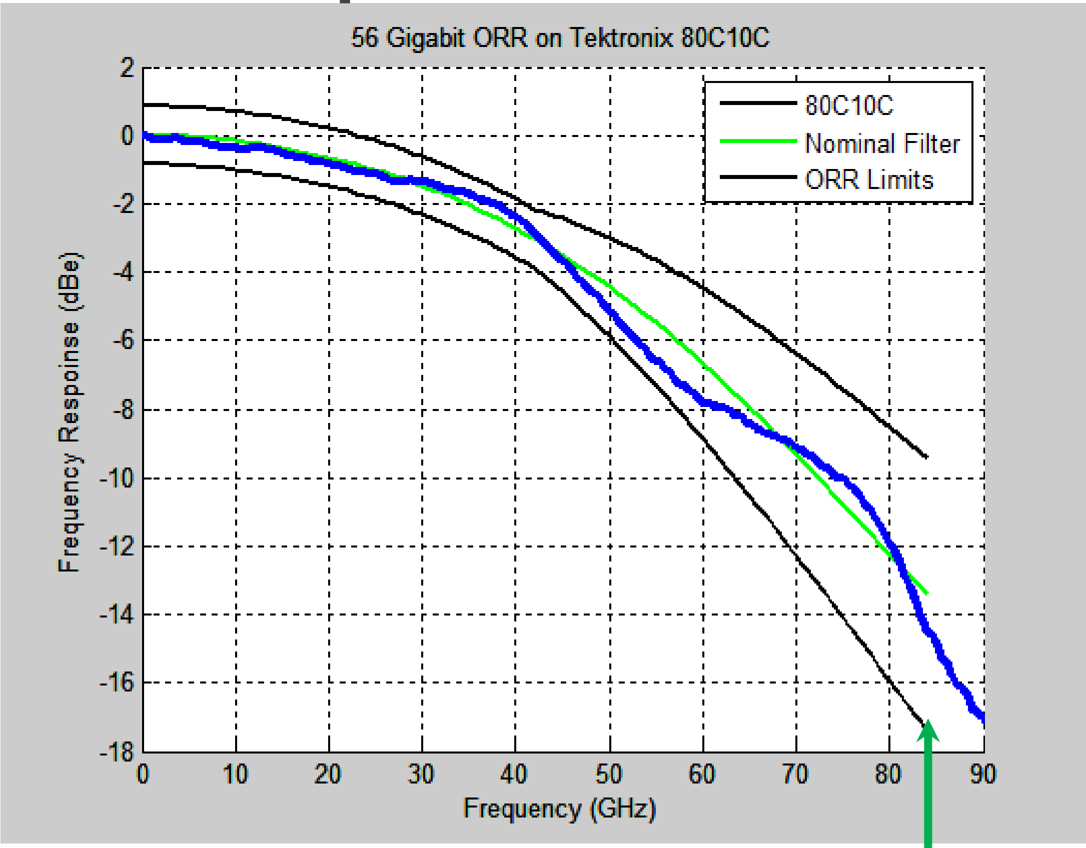
Tek 80C10C optical module:



56Gbps Optical Reference Receiver on Highest Optical Bandwidth Oscilloscope

80C10C, 80C10C-CRTP

- High sensitivity with and without CR
- Support for Optical Bessel-Thompson Filter in HW (no DSP, no special pattern needed)
- Electrical Data Out (optional) for:
  - Clock Recovery
  - Real-time oscilloscope for troubleshooting
  - BER Analysis



- Best noise performance at 40G, 56G → best system for PAM4 @ 56 GBd
- **<u>~100 GHz optical Bandwidth</u>**

Compliant @ 84 GHz !!!

Receiver Jitter and Noise decomposition detail

- Accurate jitter and noise decomposition is key to root cause analysis of Signal Integrity problems.
- Random Jitter/Noise: Caused by thermal and shot noise effects on semiconductor junctions and/or laser relative intensity noise.
- Deterministic Jitter/Noise: Contributed to by a wide set of factors ranging from non uniform channel performance or periodic signal content or cycle asymmetry.
- Total Jitter at BER (typically 1E-12, but increasingly 1E-6 with FEC) depicts the aggregate effects of all the jitter terms on eye width to user defined low probabilities. Similarly Total Noise depicts the net effects of the noise components at the same Bit Error Ratio.

Global | Eye0 | Eye1 | Eye2 | Mask

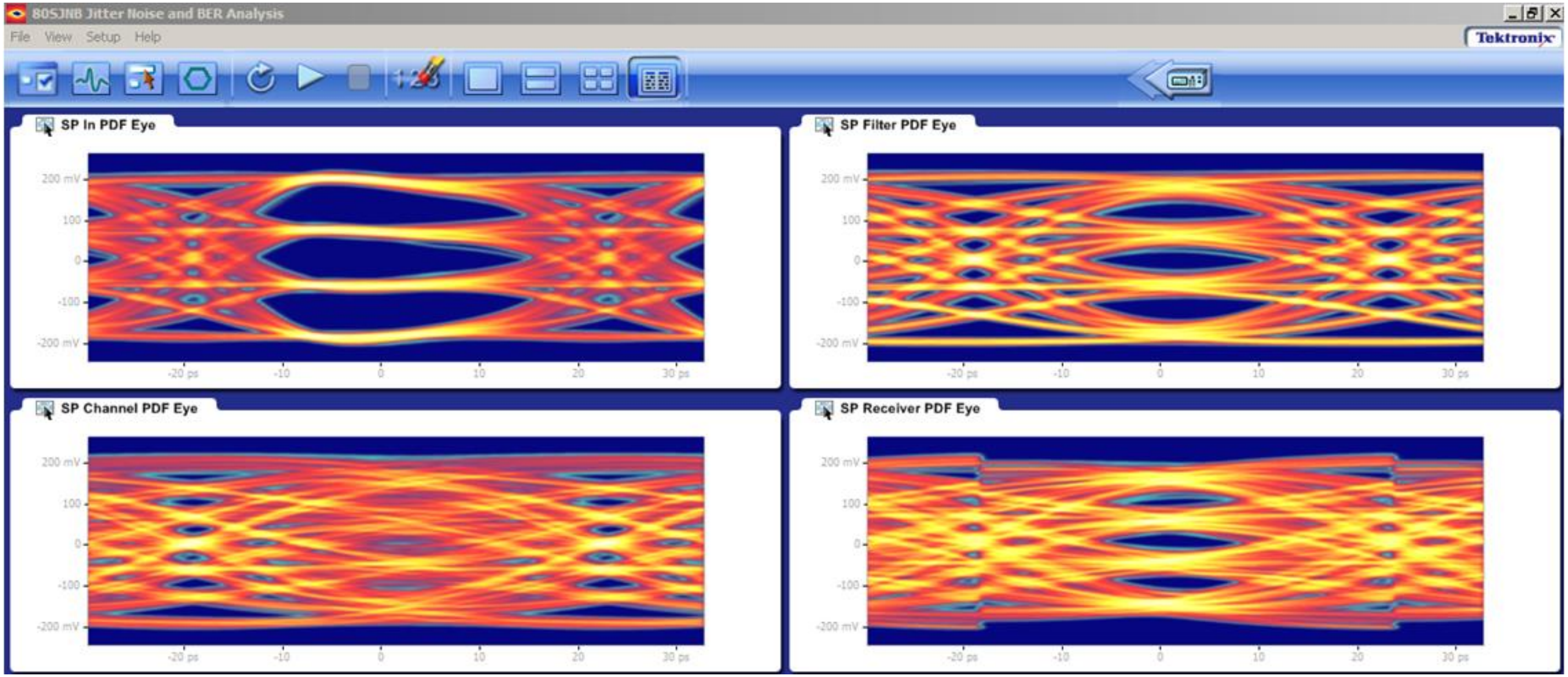
Data Source: BSA286CLand2modulators.mat	Rate: 25.78125 GBaud	Filter: True	Rx Optimizer: On
Coding: PAM	Pattern: 511 symbols	Channel: True	Rx Common Phase: False
Phase Reference: None	Sample Count: 271.10 k	Equalizer: FFE (10)	Rx Status: Optimized

Jitter (Decision Threshold: 1.1 mW)		
Random Jitter		
RJ (RMS)	=	665 fs
RJ(h) (RMS)	=	572 fs
RJ(v) (RMS)	=	340 fs
Deterministic Jitter		
DJ	=	26 ps
DDJ	=	24 ps
DCD	=	395 fs
DDPWS	=	18 ps
BUJ(d-d)	=	50 fs
PJ	=	428 fs
PJ(h)	=	425 fs
PJ(v)	=	51 fs
NPJ(d-d)	=	50 fs
Total Jitter @ BER		
TJ (1E-12)	=	32 ps
Eye Opening (1E-12)	=	6.7 ps
Additional Jitter Measurements		
J2 (2.5E-3)	=	27 ps
J9 (2.5E-10)	=	31 ps

Noise (Sampling Phase: 0.5 % UI)		
Random Noise		
RN (RMS)	=	13 uW
RN(v) (RMS)	=	13 uW
RN(h) (RMS)	=	45 pW
Deterministic Noise		
DN	=	274 uW
DDN	=	272 uW
DDN(upper)	=	228 uW
DDN(lower)	=	304 uW
BUN(d-d)	=	2.0 uW
PN	=	2.0 uW
PN(v)	=	2.0 uW
PN(h)	=	33 pW
NPN(d-d)	=	2.0 uW
Total Noise @ BER		
TN (1E-12)	=	439 uW
Eye Opening (1E-12)	=	122 uW
Eye Amplitude	=	561 uW
SSC Modulation		
Magnitude	=	0 ppm
Frequency	=	0 Hz

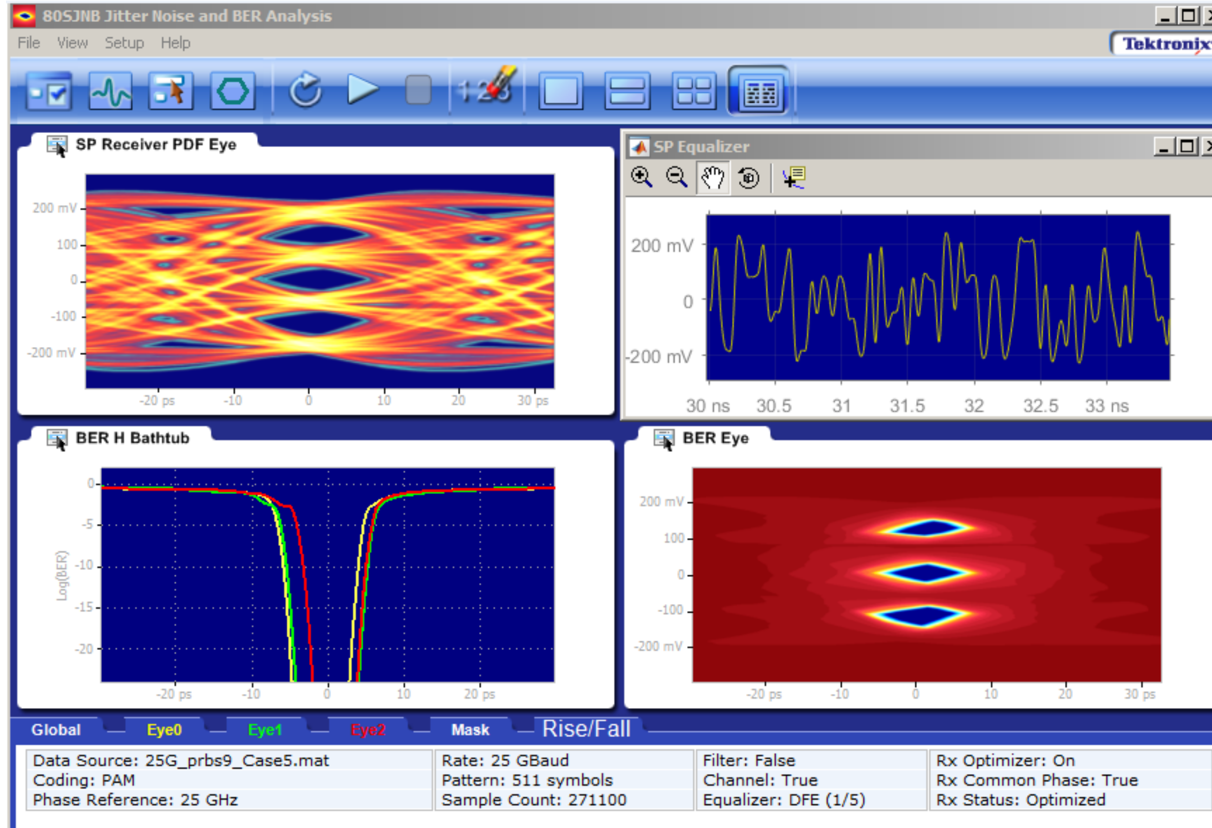
DFE with Signal Path Emulation

- Start with a near end Tx Signal.
- Right: Bandwidth compromised
- Lower Left: Interconnect emulation (via S-Parameters)
- Lower Right: Receiver compensation with a DFE (Non Linear Decision Feedback Equalizer).



PAM4 Transition Trellis table

- In the field of advanced encoding and error correction it’s valuable to verify that transition symmetry has been maintained, as well as to be able to examine individual rise and fall transition intervals specs. This is now available in ET based systems as well as RT PAM4.



Transition	Mean(μ)	StdDev(σ)	CV(σ/μ)	Min	Max	Count
0→1	17 ps	3.3 ps	0.19	12 ps	25 ps	32
0→2	19 ps	1.8 ps	0.098	15 ps	22 ps	32
0→3	19 ps	1.3 ps	0.067	17 ps	22 ps	32
1→0	20 ps	2.5 ps	0.12	16 ps	29 ps	32
1→2	19 ps	3.7 ps	0.19	12 ps	29 ps	32
1→3	20 ps	1.5 ps	0.074	17 ps	23 ps	32
2→0	20 ps	1.6 ps	0.081	16 ps	23 ps	32
2→1	18 ps	2.4 ps	0.13	14 ps	24 ps	32
2→3	20 ps	2.7 ps	0.14	14 ps	27 ps	32
3→0	19 ps	962 fs	0.050	17 ps	21 ps	32
3→1	19 ps	1.7 ps	0.090	16 ps	22 ps	32
3→2	18 ps	4.0 ps	0.23	11 ps	26 ps	32

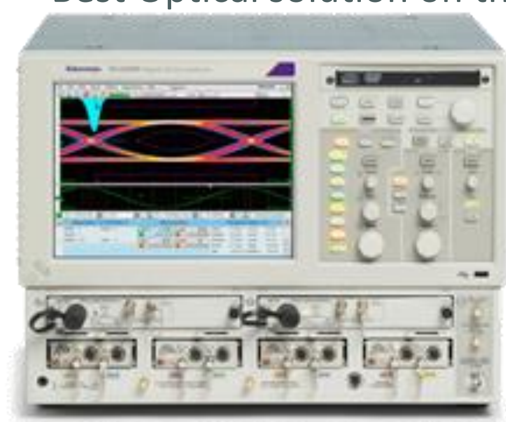
Tektronix 100G/400G Signal Acquisition Systems

Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis

- **Two world class acquisition systems cover the breadth of any 400G Verification and design needs, with the lowest noise, highest bandwidth in the industry**
  - Real Time (70GHz ATI) single shot acquisition and triggering capabilities are key tools for advanced analysis and debug.
  - Equivalent Time low noise, high sensitivity tools enable the best margin in product and device characterization.

- Real Time
  - 70GHz Analog Bandwidth, 4.3ps rise time (20%-80%)
  - 200GS/s Sample Rate
  - <125fs jitter noise floor
  - ≥25GHz Edge trigger bandwidth
  - Compact 5 ¼” Oscilloscope package
  - No physical clock recovery required (key to 400G)
  - Comprehensive CTLE, DFE, FFE signal processing
  - Lowest noise real time acquisition system
  - Best Electrical solution on the planet

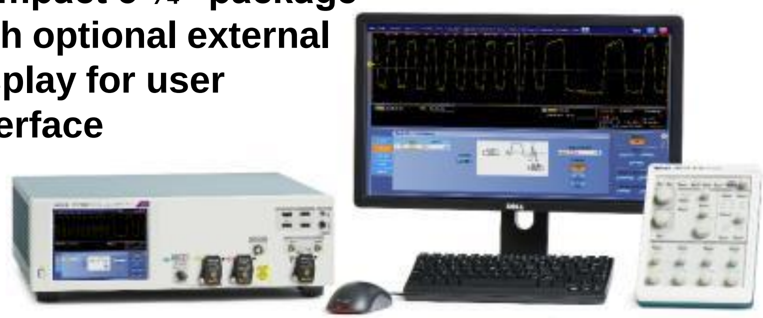
- Equivalent Time
  - 85GHz Optical Bandwidth
  - 70GHz Electrical Bandwidth
  - <100fs jitter noise floor
  - 20nW to .6uW Optical Resolution.
  - Automated test of 80 Industrial Stds.
  - Best Optical solution on the planet



Scalable Performance

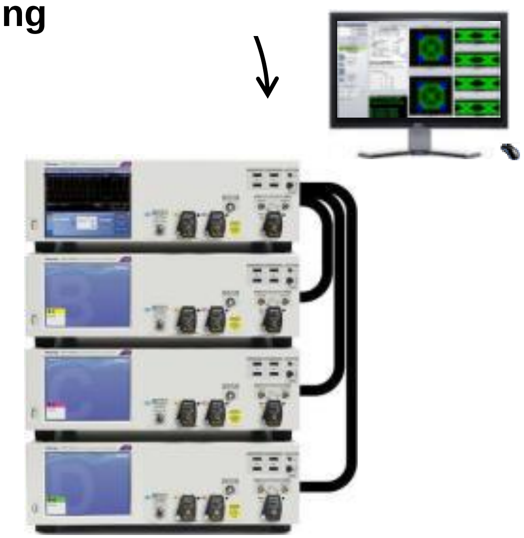
- Compact instrument for increased configuration flexibility
- UltraSync high performance synchronization for multi-unit configurations

Compact 5 ¼" package with optional external display for user interface



Additional performance using multiple units

Configuration flexibility with precisely-synchronized timing



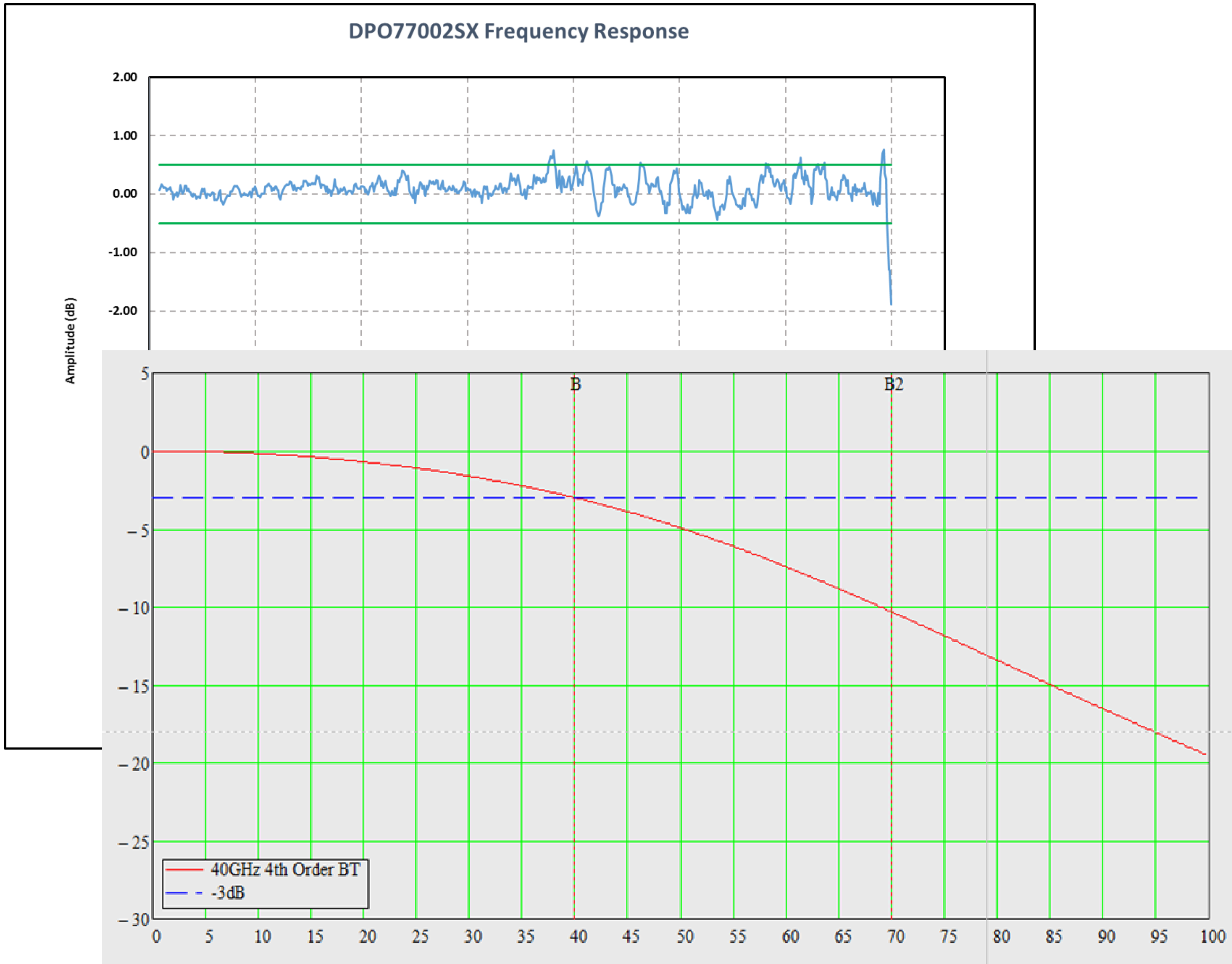
UltraSync High Performance Synchronization & Control bus

- 12.5 GHz Sample Clock Reference
- Coordinated Trigger
- High speed data path
- 2X 70GHz channels
- 4X 33GHz channels

Tektronix DPO77002SX Frequency Response

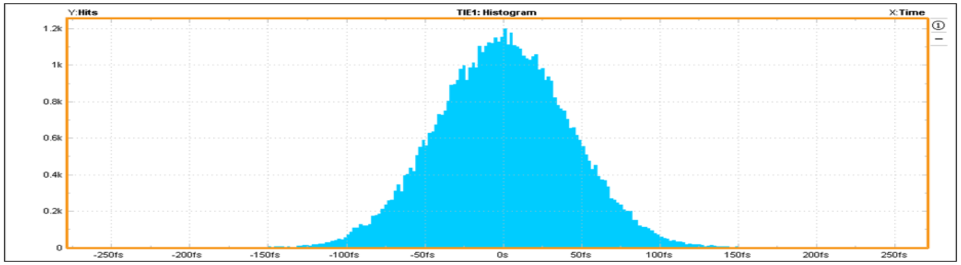
Flat intermodulation overlap zone offers the cleanest, low noise acquisition system available today.

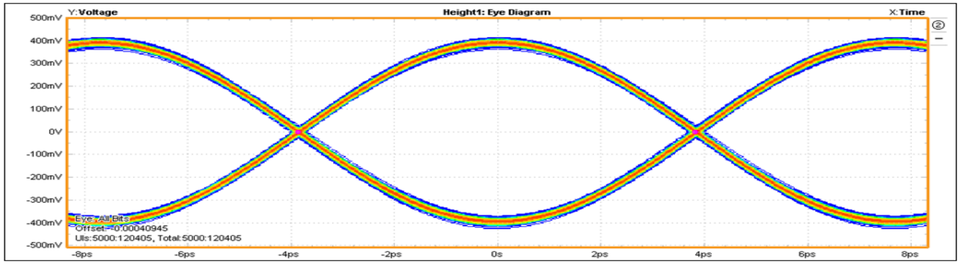
Bandwidth to 70GHz can be channel modeled in DSP to map precisely to the 40G Bessel Thompson response required by OIF-CEI physical layer measurements today.



Tektronix 100G/400G Signal Acquisition Systems

Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis





Real Time

- Multi channel time synchronized operation.
- Advanced analysis CTLE/DFE and Complex Math.
- Complex modulation analysis tools.
- Unprecedented jitter noise floor.
  - ~ 40fs RMS clock jitter 64 GHz clock)
  - <125fs jitter noise floor (64Gbps PRBS)

Measurement Results

Hide Current Aquisitions | Summary View

Description	Mean	Std Dev	Max	Min
TIE1, Math4	4.4985as	41.903fs	159.37fs	-167.66fs
Current Acquisition	4.4985as	41.903fs	159.37fs	-167.66fs
Height1, Math4	729.78mV	0.0000V	729.78mV	729.78mV
Current Acquisition	729.78mV	0.0000V	729.78mV	729.78mV
TJ@BER1, Math4	573.74fs	0.0000s	573.74fs	573.74fs
Current Acquisition	573.74fs	0.0000s	573.74fs	573.74fs
RJ–δδ1, Math4	38.441fs	0.0000s	38.441fs	38.441fs
Current Acquisition	38.441fs	0.0000s	38.441fs	38.441fs
DJ–δδ1, Math4	35.570fs	0.0000s	35.570fs	35.570fs
Current Acquisition	35.570fs	0.0000s	35.570fs	35.570fs
Width@BER1, Math4	14.811ps	0.0000s	14.811ps	14.811ps
Current Acquisition	14.811ps	0.0000s	14.811ps	14.811ps
PJ1, Math4	80.938fs	0.0000s	80.938fs	80.938fs
Current Acquisition	80.938fs	0.0000s	80.938fs	80.938fs
DJ1, Math4	83.367fs	0.0000s	83.367fs	83.367fs
Current Acquisition	83.367fs	0.0000s	83.367fs	83.367fs
RJ1, Math4	38.441fs	0.0000s	38.441fs	38.441fs
Current Acquisition	38.441fs	0.0000s	38.441fs	38.441fs
DDJ1, Math4	0.0000s	0.0000s	0.0000s	0.0000s
Current Acquisition	0.0000s	0.0000s	0.0000s	0.0000s

Source Reference Levels

Source	Autoset Method	Rise High	Rise Mid	Rise Low
Ch1	Auto	70.16mV	400uV	-69.36mV
Ch2	Auto	-44.04mV	-114.6mV	-185.16mV
Ch3	Auto	1V	0V	-1V
Ch4	Auto	1V	0V	-1V
Math1	Auto	1V	0V	-1V
Math2	Auto	-80.697mV	-302mV	-523.31mV
Math3	Auto	209.4mV	982.61uV	-207.43mV
Math4	Auto(Low-High(full wfm))	308.9mV	-409.45uV	-309.72mV
Ref1	Auto	1V	0V	-1V
Ref2	Auto	1V	0V	-1V
Ref3	Auto	1V	0V	-1V
Ref4	Auto	1V	0V	-1V

Miscellaneous Settings

	Gating	Qualify	Population
State	Cursors	Off	Off
Source	--	--	--
Size	--	--	--

Pattern Length

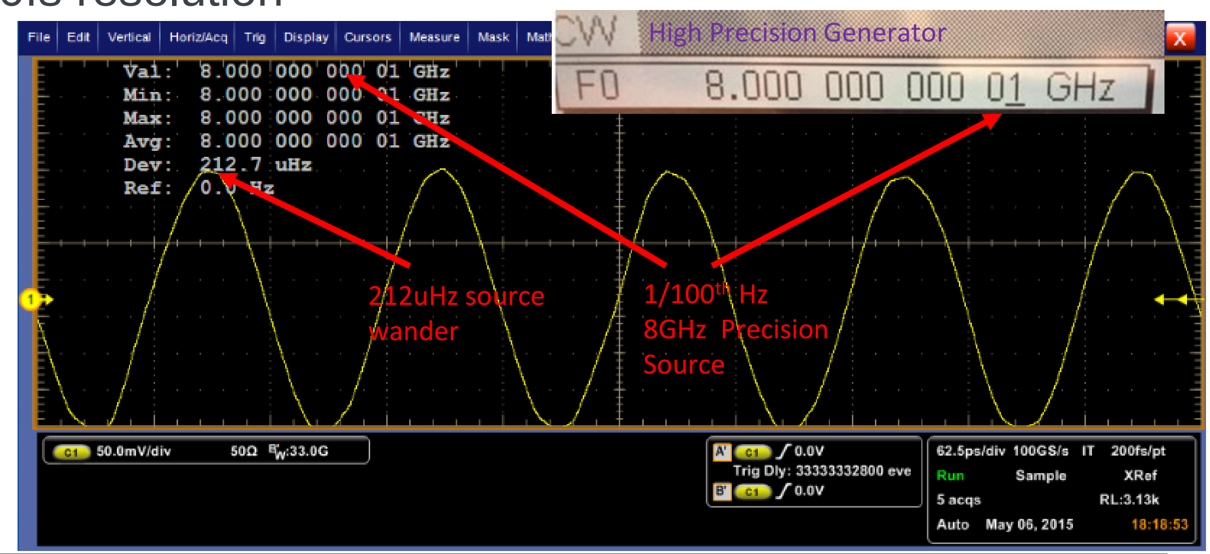
Source	Data Rate	Pattern Type	Pattern Length
MATH4	130.00Gb/s	Repeating	2UI

Tektronix 100G/400G Signal Acquisition Systems

Equivalent Time Signal Acquisition • Real Time Signal Acquisition Software Control and Analysis

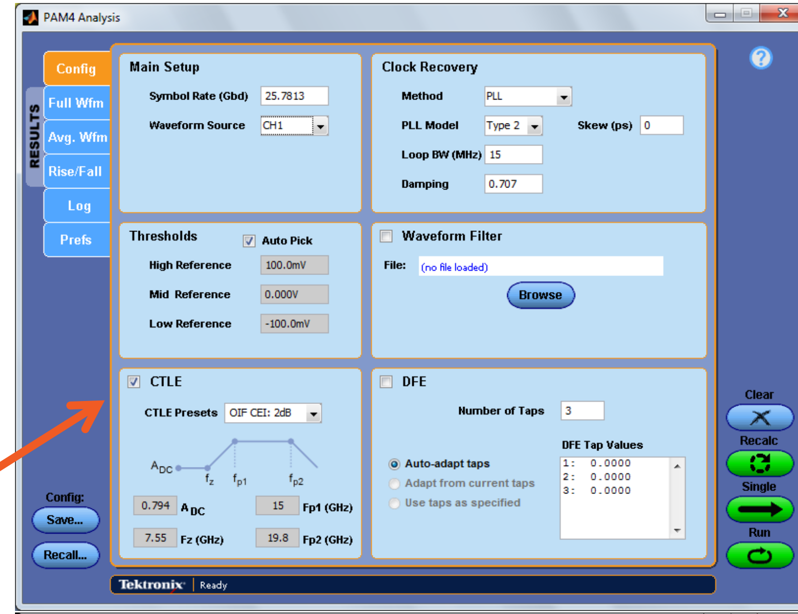
Real Time

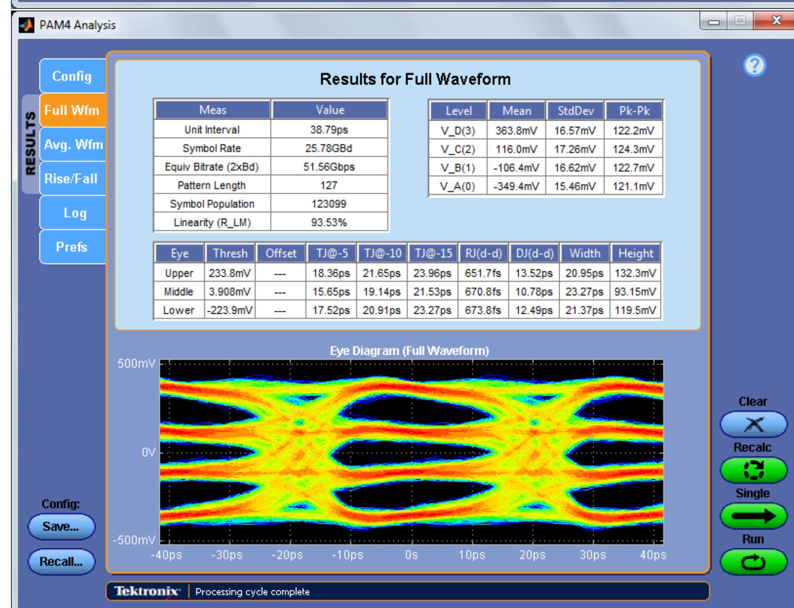
- New HW trigger performance level easily triggers on 100G tributary Runt
- New Internal 13-digit precision frequency counter (54bit) provides frequency analysis to 25GHz, with 200fs resolution
- Highly accurate clock stability measurements
- Accurate to < 1 part per billion



Real-Time PAM4

- PAM4 Analysis is a new application for real time oscilloscopes.
- It leverages DPOJET for eye diagrams and jitter decomposition.
- Full DSP based Clock Recovery and Signal Analysis up to 112Gbps/56GBaud signal rates.
- Configurability
  - PLL or Explicit clock recovery
  - Adjustable or automatic thresholds
  - Filter insertion (e.g. for de-embedding probes or cables)
  - CTLE (full custom or presets)
  - DFE
- Measurements
  - Full waveform
    - EH/EW at BER
    - Linearity
    - Jitter extrapolation at BER
  - Correlated (averaged) waveform
  - Rise / Fall per each transition type





Results for Full PAM4 Waveform

PAM4 Analysis

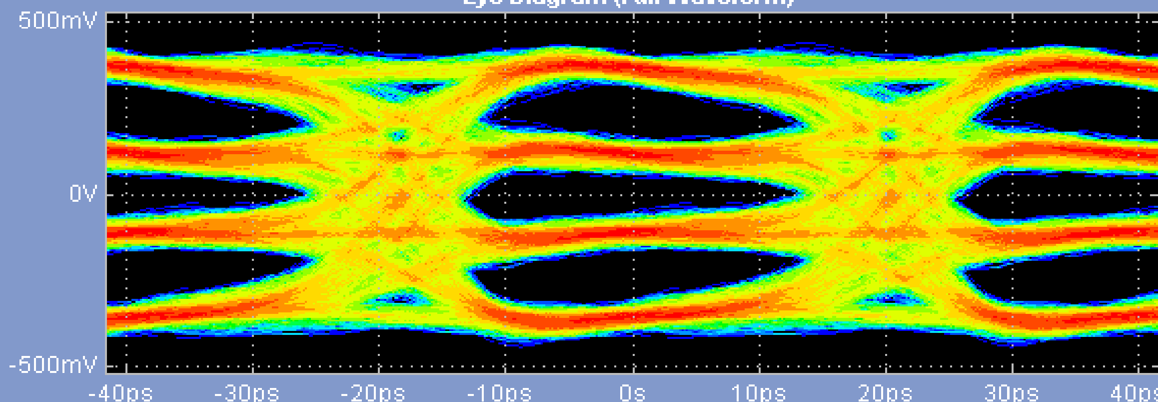
Results for Full Waveform

Meas	Value
Unit Interval	38.79ps
Symbol Rate	25.78GBd
Equiv Bitrate (2xBd)	51.56Gbps
Pattern Length	127
Symbol Population	123099
Linearity (R_LM)	93.53%

Level	Mean	StdDev	Pk-Pk
V_D(3)	363.8mV	16.57mV	122.2mV
V_C(2)	116.0mV	17.26mV	124.3mV
V_B(1)	-106.4mV	16.62mV	122.7mV
V_A(0)	-349.4mV	15.46mV	121.1mV

Eye	Thresh	Offset	TJ@-5	TJ@-10	TJ@-15	RJ(d-d)	DJ(d-d)	Width	Height
Upper	233.8mV	---	18.36ps	21.65ps	23.96ps	651.7fs	13.52ps	20.95ps	132.3mV
Middle	3.908mV	---	15.65ps	19.14ps	21.53ps	670.8fs	10.78ps	23.27ps	93.15mV
Lower	-223.9mV	---	17.52ps	20.91ps	23.27ps	673.8fs	12.49ps	21.37ps	119.5mV

Eye Diagram (Full Waveform)



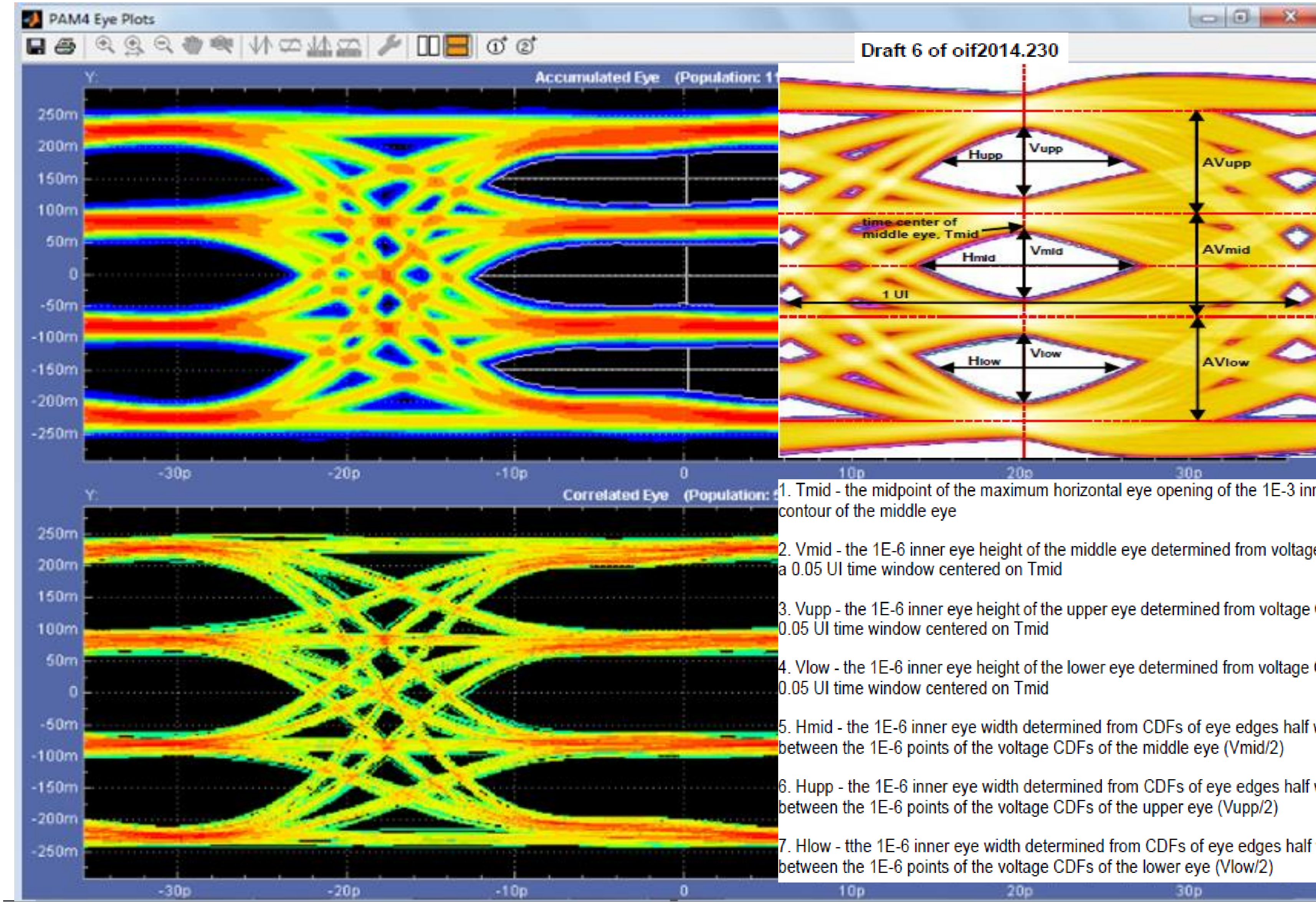
RESULTS: Config | Full Wfm | Avg. Wfm | Rise/Fall | Log | Prefs

Config: Save... Recall...

Clear | Recalc | Single | Run

Tektronix | Processing cycle complete

Eye Height at BER (Noise Decomp), Tmid, Vmid



1. Tmid - the midpoint of the maximum horizontal eye opening of the 1E-3 inner eye contour of the middle eye

2. Vmid - the 1E-6 inner eye height of the middle eye determined from voltage CDFs in a 0.05 UI time window centered on Tmid

3. Vupp - the 1E-6 inner eye height of the upper eye determined from voltage CDFs in a 0.05 UI time window centered on Tmid

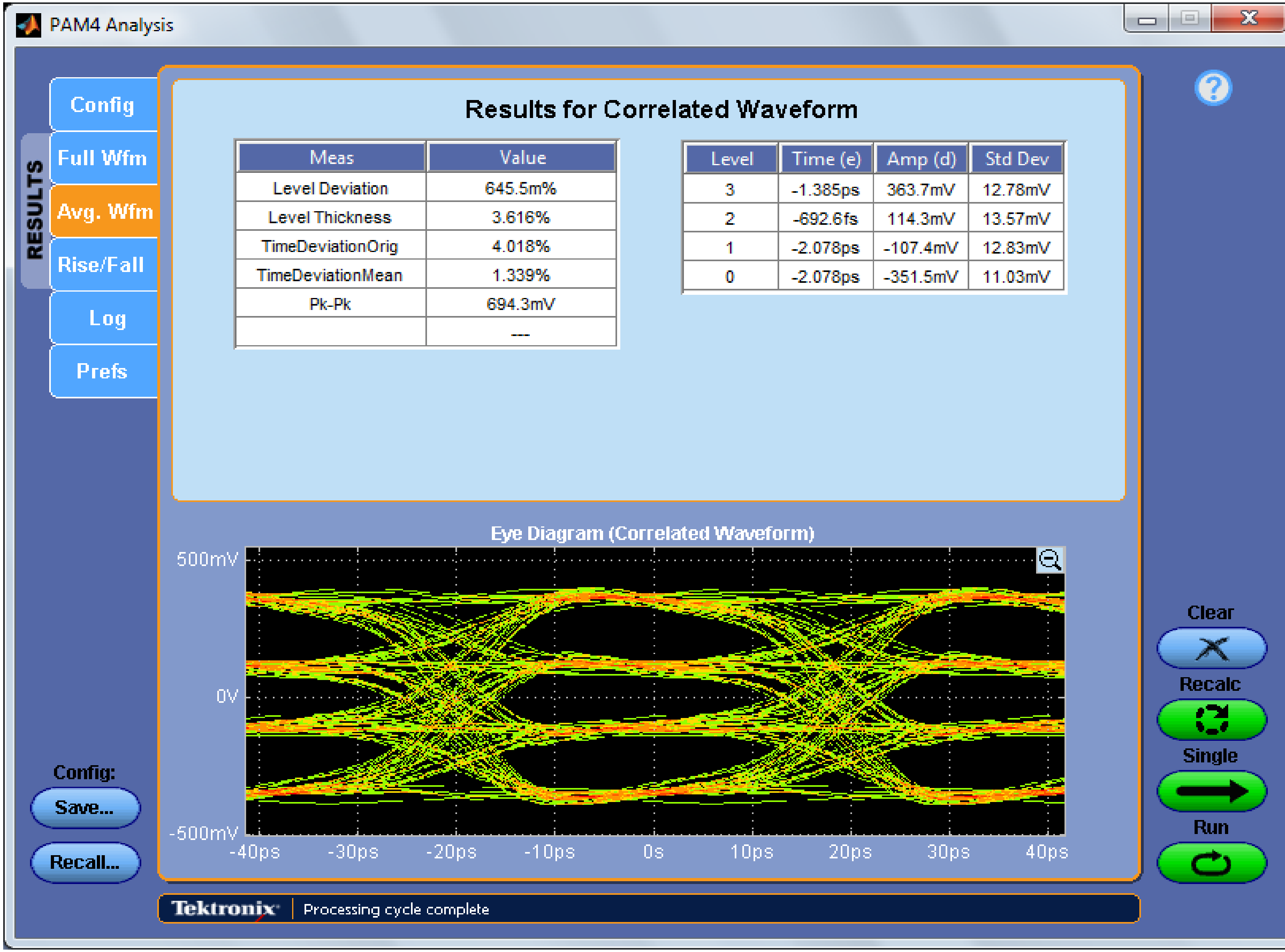
4. Vlow - the 1E-6 inner eye height of the lower eye determined from voltage CDFs in a 0.05 UI time window centered on Tmid

5. Hmid - the 1E-6 inner eye width determined from CDFs of eye edges half way between the 1E-6 points of the voltage CDFs of the middle eye (Vmid/2)

6. Hupp - the 1E-6 inner eye width determined from CDFs of eye edges half way between the 1E-6 points of the voltage CDFs of the upper eye (Vupp/2)

7. Hlow - tthe 1E-6 inner eye width determined from CDFs of eye edges half way between the 1E-6 points of the voltage CDFs of the lower eye (Vlow/2)

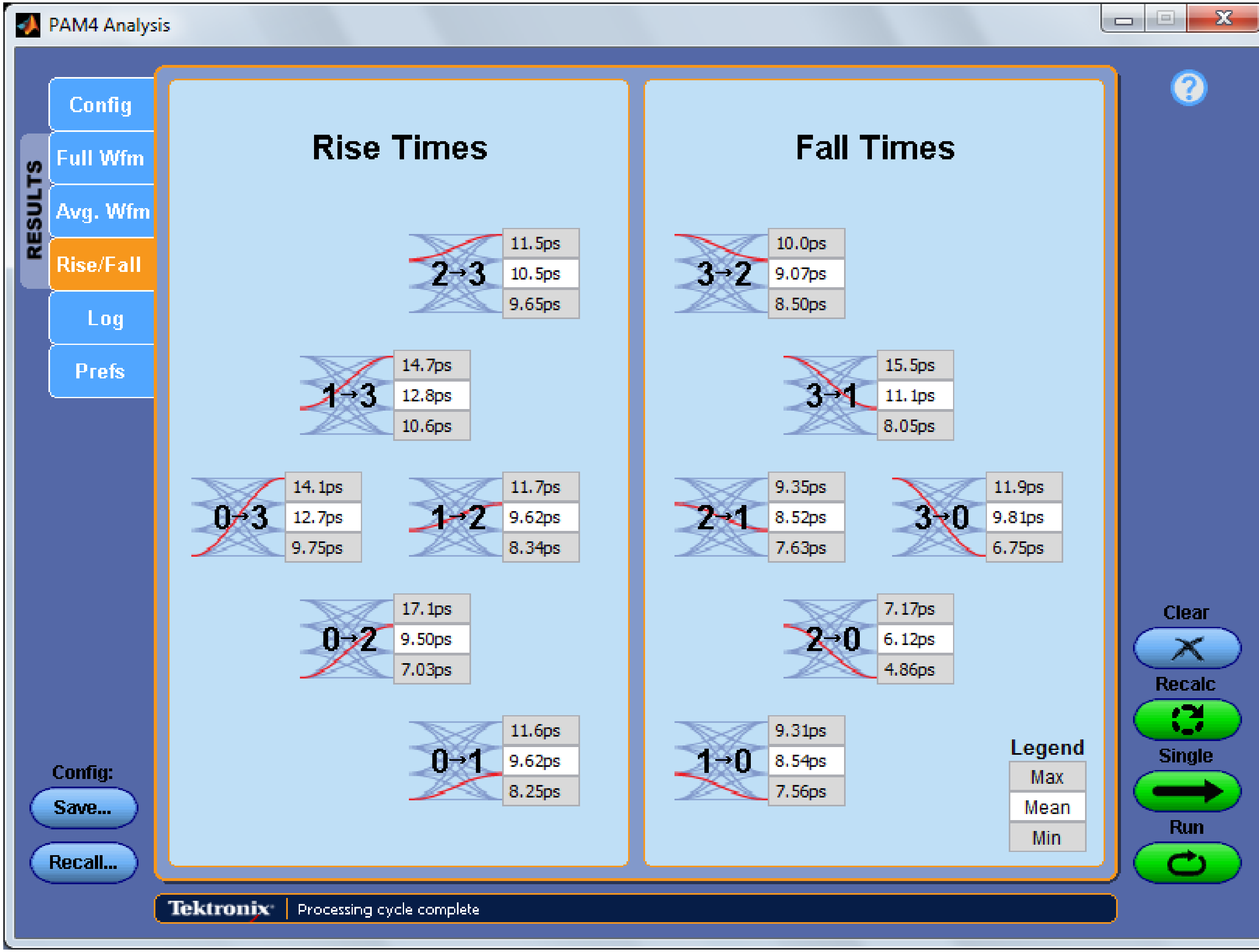
Results for Correlated (Averaged) PAM4 Waveform



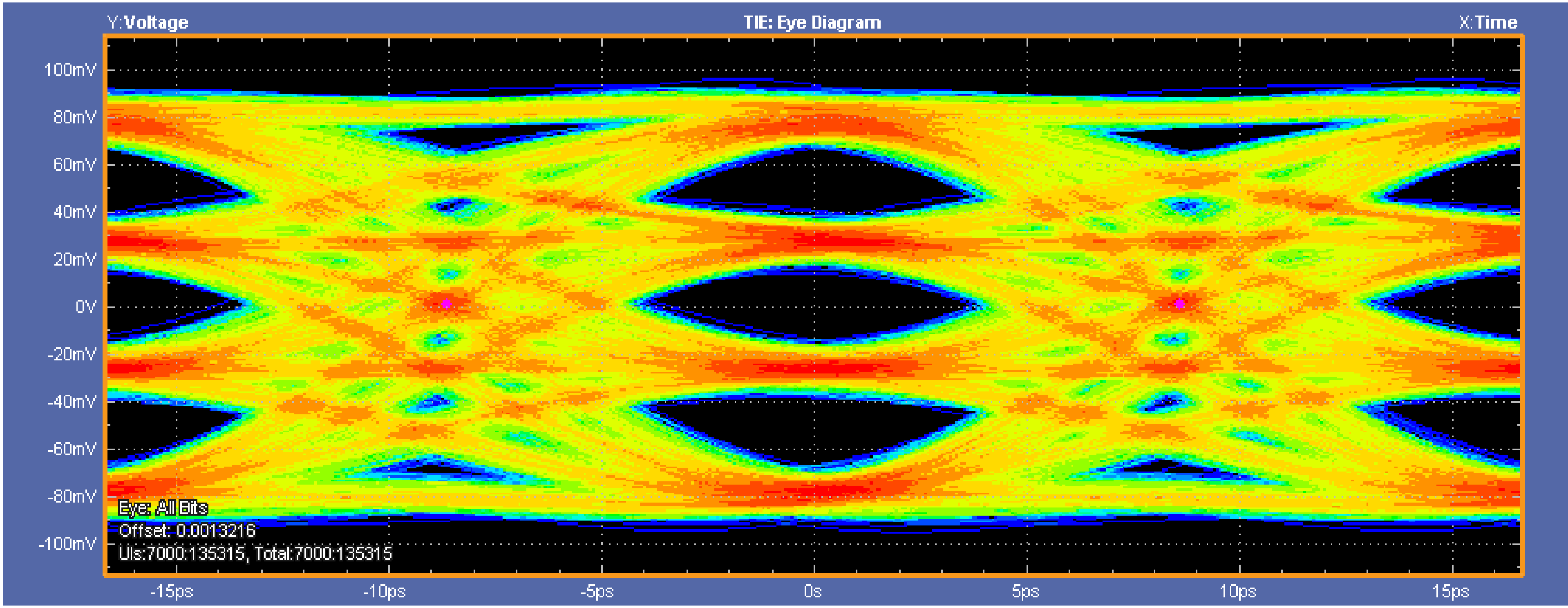
Meas	Value
Level Deviation	645.5m%
Level Thickness	3.616%
TimeDeviationOrig	4.018%
TimeDeviationMean	1.339%
Pk-Pk	694.3mV

Level	Time (e)	Amp (d)	Std Dev
3	-1.385ps	363.7mV	12.78mV
2	-692.6fs	114.3mV	13.57mV
1	-2.078ps	-107.4mV	12.83mV
0	-2.078ps	-351.5mV	11.03mV

Results: PAM4 Rise Time / Fall Time Analysis



56GBaud PAM4 (112Gbit) Setup (400GBASE-DR4)



Measurement	Value
Unit Interval	17.24ps
Symbol Rate	58.00GBd
Equiv Bitrate (2xBd)	116.0Gbps
Pattern Length	127
Symbol Population	135327
Linearity (R_LM)	97.70%

Eye	Thresh	Offset	TJ@-5	TJ@-10	TJ@-15	RJ(d-d)	DJ(d-d)	Width
Upper	45.84mV	-1.907ps	14.10ps	16.64ps	18.37ps	466.1fs	10.86ps	2.726ps
Middle	1.252mV	-2.050ps	12.62ps	14.82ps	16.30ps	388.9fs	10.02ps	4.098ps
Lower	-44.43mV	-2.350ps	14.19ps	16.57ps	18.17ps	427.3fs	11.28ps	3.253ps

Level	Mean	StdDev	Pk-Pk
V_D(3)	68.29mV	5.689mV	34.93mV
V_C(2)	24.16mV	5.789mV	37.65mV
V_B(1)	-22.37mV	5.952mV	38.39mV
V_A(0)	-67.23mV	5.913mV	39.95mV

400G Summary

- PAM4 (Higher order Modulation) technology is a major inflection point in the next increase of data-rate to 400G. Measurement specs for PAM4 are in flux, and it's important to stay current on measurement techniques being formalized by the standards.

- Be mindful of the Bessel Thompson roll off behavior of the bandwidth specifications. These typically constrain channels out to their 10dB point (1.5X symbol rate) which can range from 50-70GHz electrically and up to 84GHz optically

- Solutions for 400G should address both 28GBaud and 56GBaud. Ideal solutions should be able to support both.

- Current technology (80C10C) offers separate option for near 100GHz Performance for technology research, as well as an option which supports all ORR filters from 25-56GBaud as a true analog HW filter.