TEK Talks -
決勝行動高速介面量測新戰場

Tektronix®

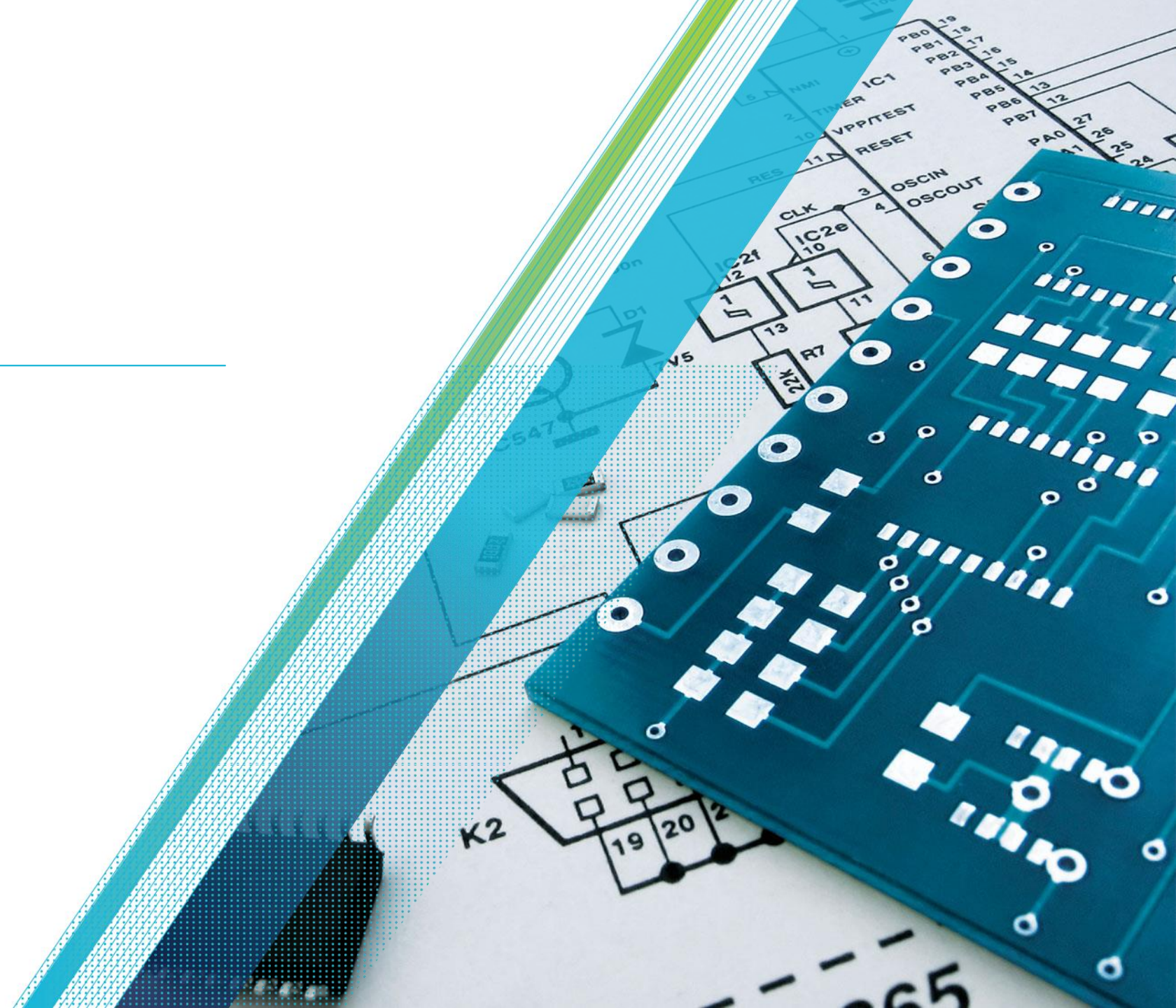
Tektronix

HDMI and DisplayPort

(MTE event, Taiwan)

Yogesh Pai & Brian Chen

31 MARCH 2016

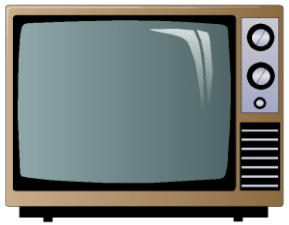


Agenda

- Display Ecosystem Updates
- DisplayPort
  - Technology and Trends
  - Measurement Challenges
  - Tektronix Solution
- HDMI
  - Technology and Trends
  - Measurement Challenges
  - Tektronix Solution
- General Q and A session

Display Ecosystem

1985-1995
VGA



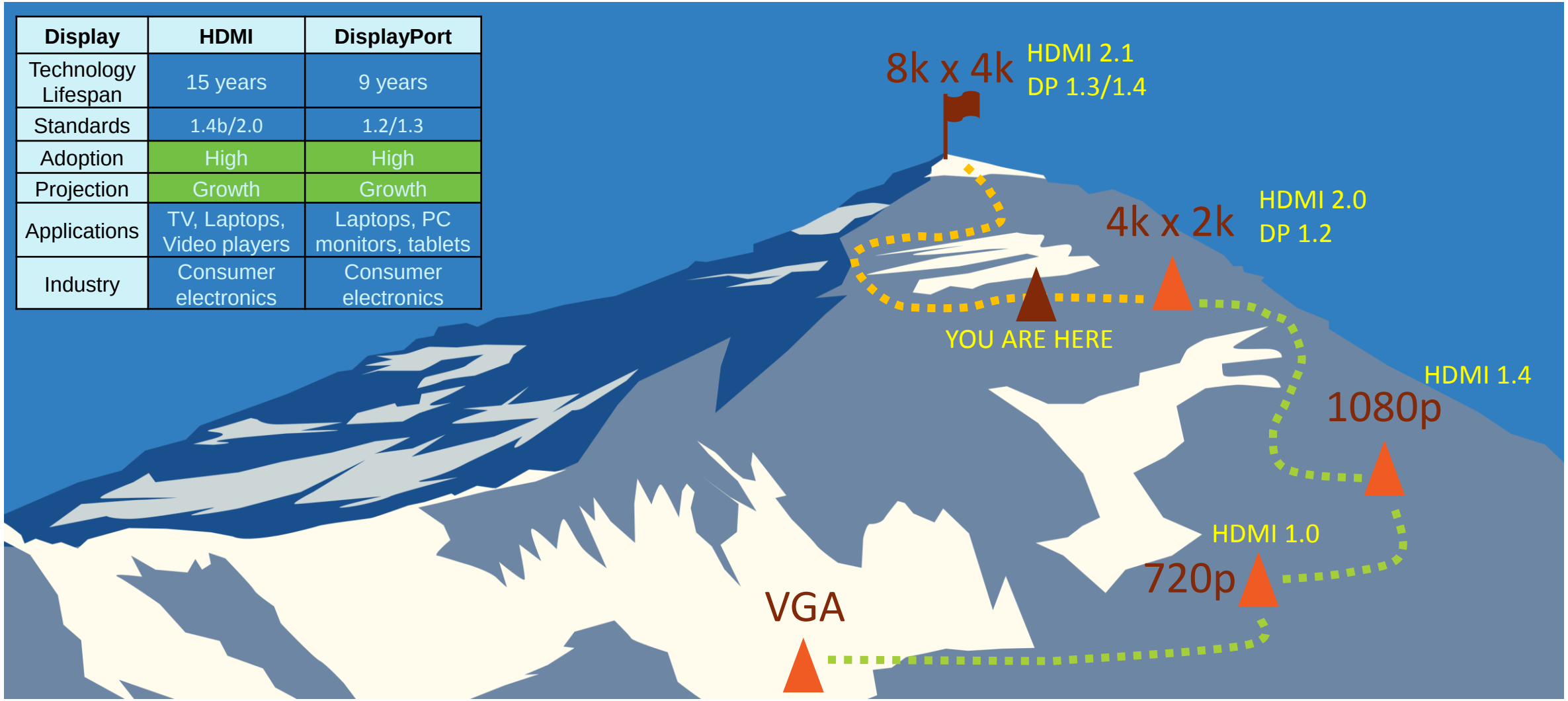
1995-2002
DVI

2003-2015
HDMI (HDMI 1.4/2.0) **DP** (1.2)

FUTURE
HDMI (HDMI 2.1) **DP** (1.3)

Technology Roadmap

Display	HDMI	DisplayPort
Technology Lifespan	15 years	9 years
Standards	1.4b/2.0	1.2/1.3
Adoption	High	High
Projection	Growth	Growth
Applications	TV, Laptops, Video players	Laptops, PC monitors, tablets
Industry	Consumer electronics	Consumer electronics



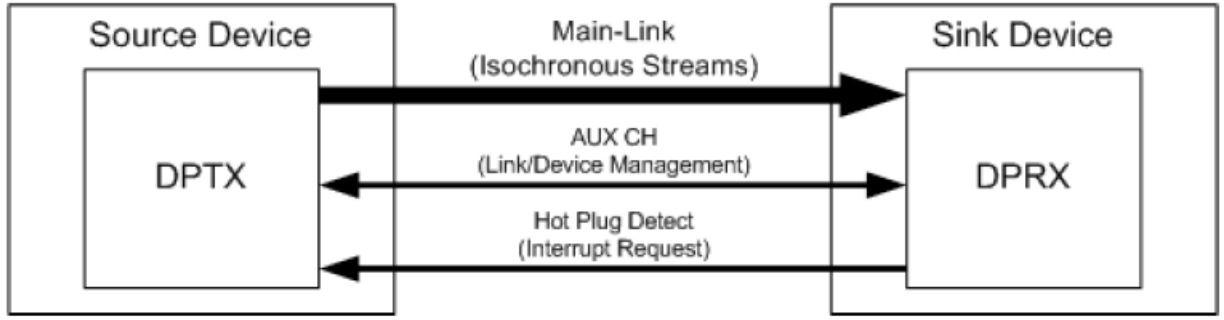
Display Ecosystem Activities

- Consortium Workgroup Participation:
  - HDMI TWG/TSG/PHY (Vasudev is now in the BoD of HDMI Forum)
  - DP on USB-C Subgroup
  - DP PHY Electrical Subgroup
  - MHL CTS engagement with Lattice team
- Ecosystem Events:
  - HDMI MOI approval events
  - HDMI Face to Face events
  - CEA plugtest
  - DisplayPort plugtest

DisplayPort

Technology Overview

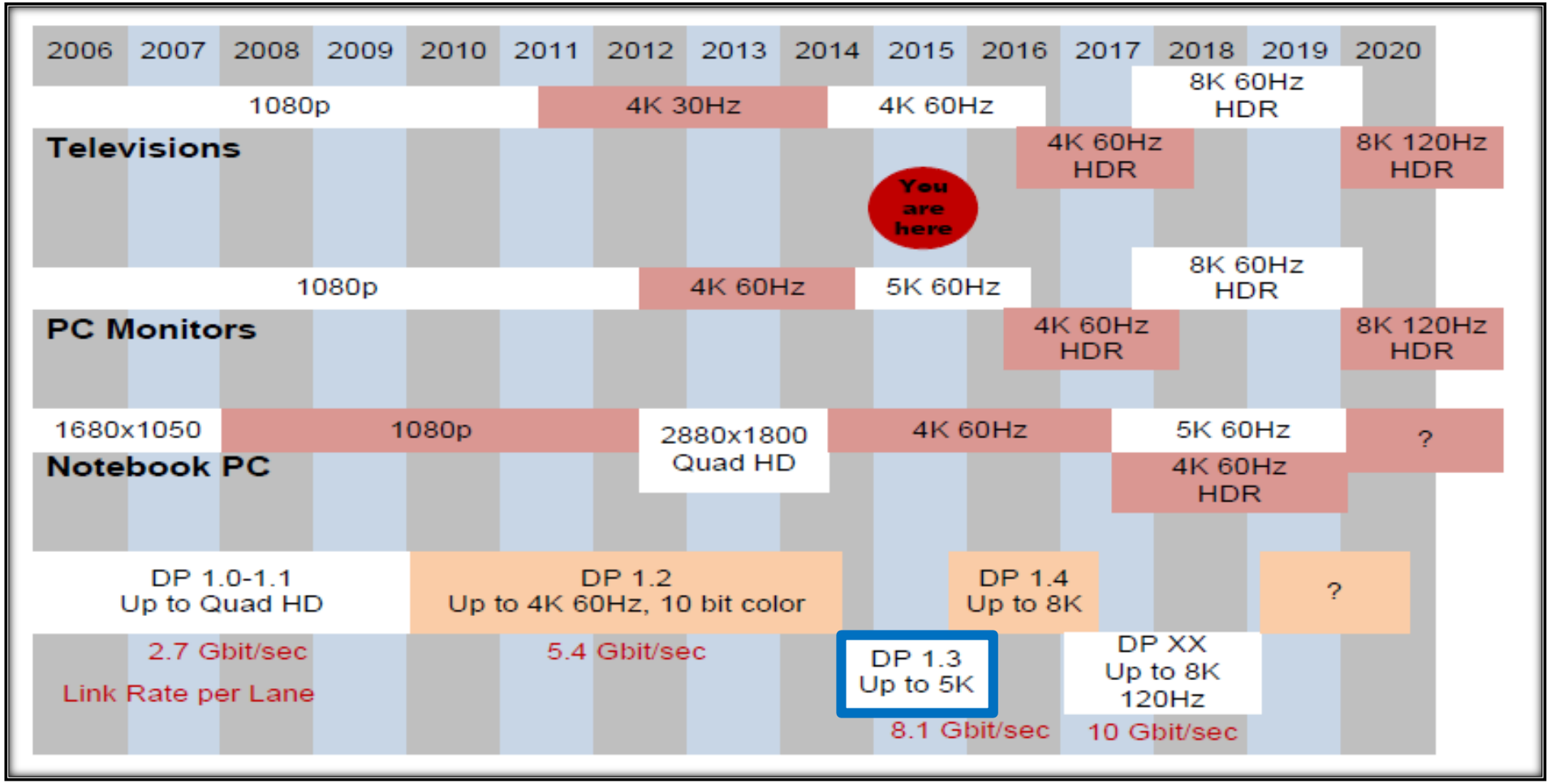
- Main-Link
  - Unidirectional, high-bandwidth, low-latency channel
  - Transports uncompressed video and audio
- Auxiliary channel
  - Half-duplex, bidirectional channel
  - Link management and device control
- Hot Plug Detect (HPD) signal line
  - Serves as an interrupt request by the Sink device



DisplayPort Standards

- Standard DisplayPort
  - Specification Version 1.3/CTS Version (Expected Q3 - 2016)
  - Data Rates 1.62GBps, 2.7Gbps, 5.4Gbps and **8.1Gbps**
- Alt Mode on USB Type-C *(latest)*
  - Specification Version 1.0 (Spec 2014)/CTS draft stage
- eDP
  - Specification Version 1.4a/ CTG draft stage – would support 8.1Gbps
  - Embedded (single box – Laptops) (1,2,4 lanes)
- MyDP
  - Specification Version 1.0/ CTS Version 1.0
  - Data Rates 1.62GBps, 2.7Gbps and 5.4Gbps
  - Mobiles (1 lane)

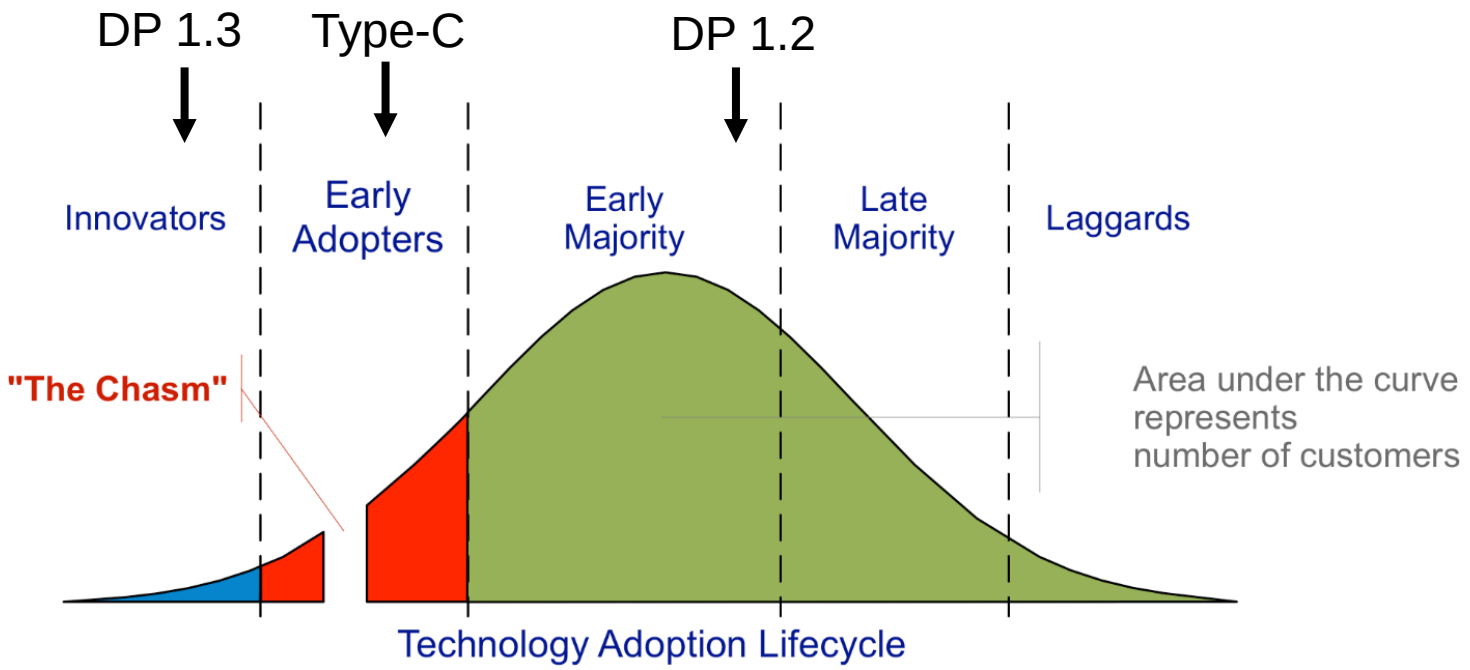
Technology Roadmap



Source : **VESA**

DisplayPort

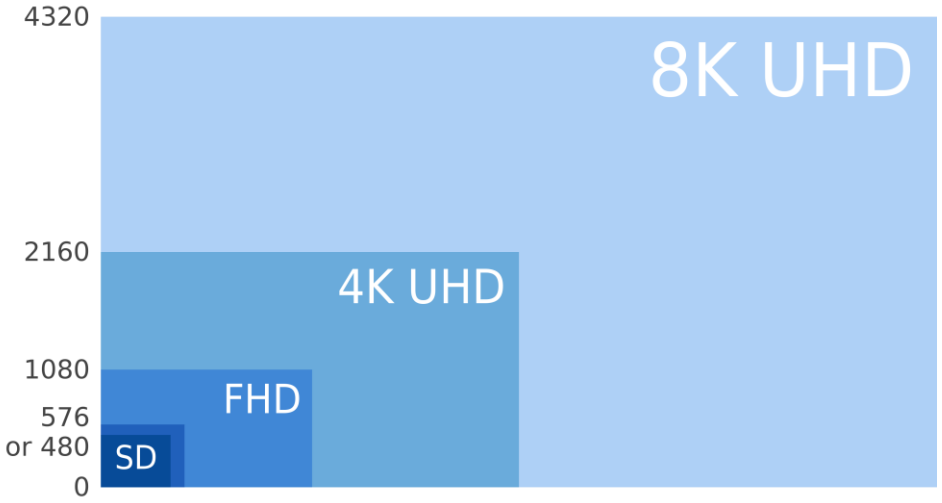
TECHNOLOGY AND TRENDS



- DP 1.2 is in mainstream products today; Highest speed 5.4 Gbps
- DP 1.3 is in early CTS draft stage; Highest speed 8.1 Gbps

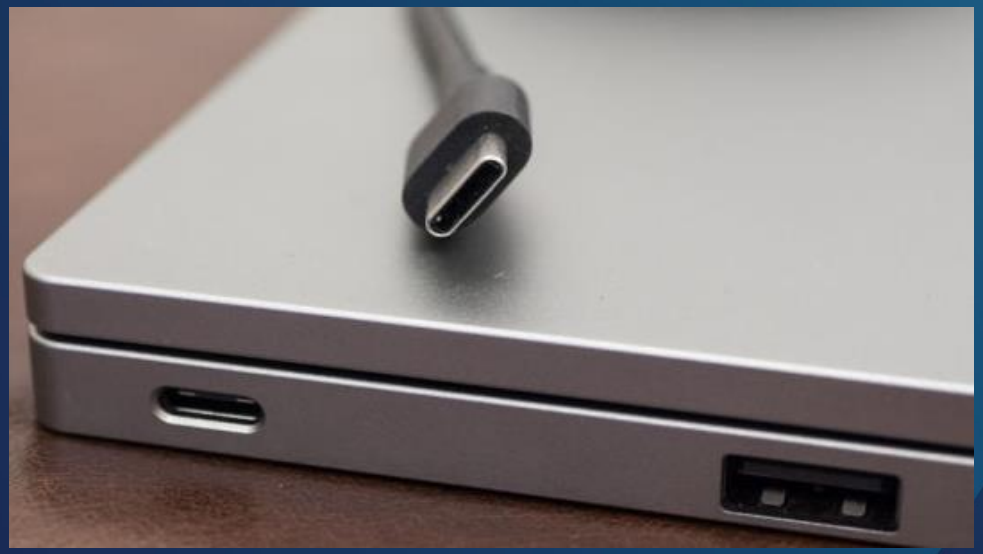
Technology Updates – DP 1.3 Link rate

DP Version Introduction	Link Rate Name	Bit rate	Max Resolution Support (24 bpp, 60Hz Refresh, 4:4:4 format)	Max Resolution Support (24 bpp, 60Hz Refresh, 4:2:0 format)
DP 1.0	RBR	1.62 Gbps	1920x1080	Not supported
	HBR	2.7 Gbps	2560x1600	Not supported
DP 1.2	HBR2	5.4 Gbps	4K x 2K	Not supported
DP 1.3	HBR3	8.1 Gbps	5K x 3K	8K x 4K

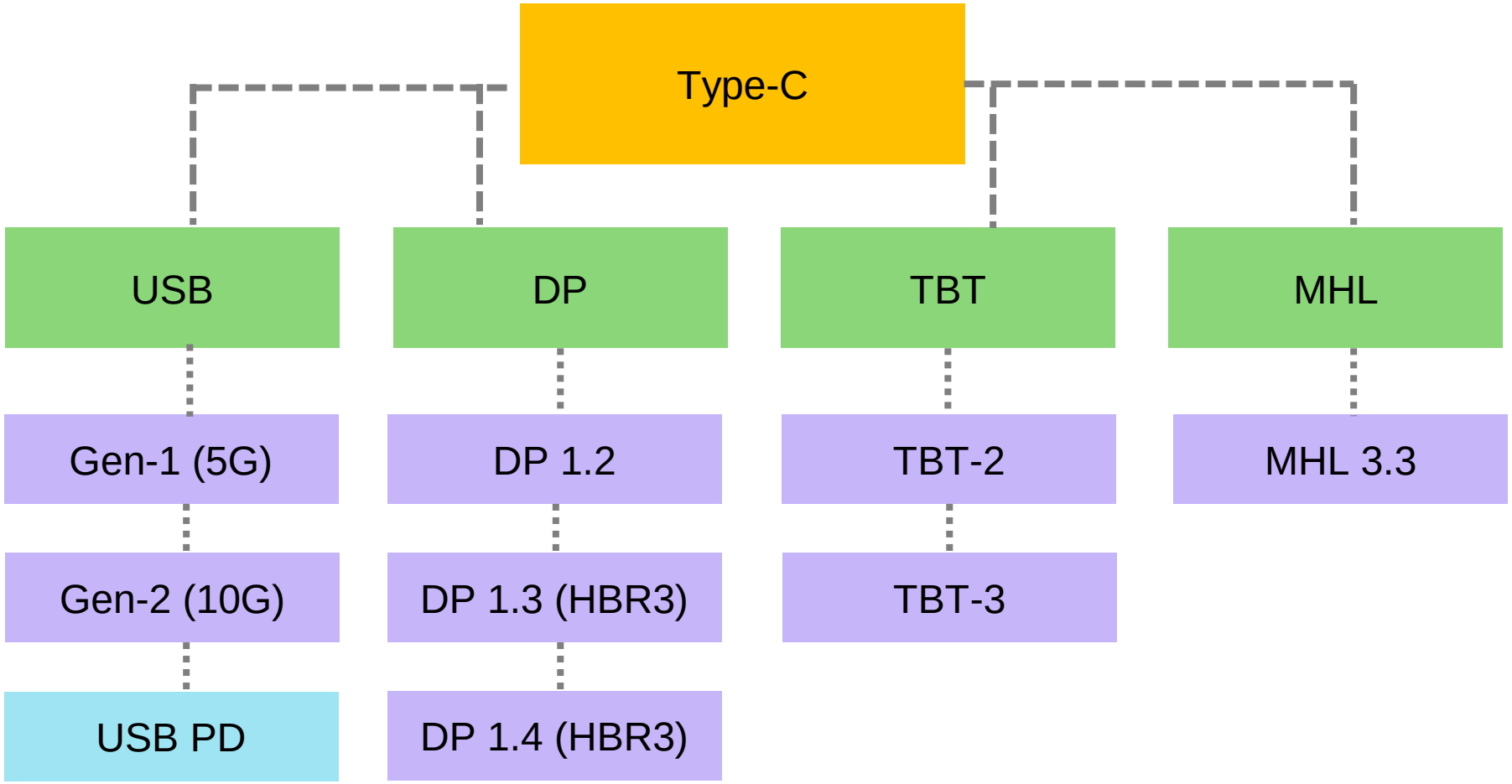


- Total useable data transfer rate for DP 1.3 → 25.92 Gbps
- Higher Bandwidth
  - Higher resolution
  - Deeper colors
  - Higher refresh rates

DisplayPort Alternate Mode on USB Type-C



Type-C Solution Overview



The USB Type-C connector

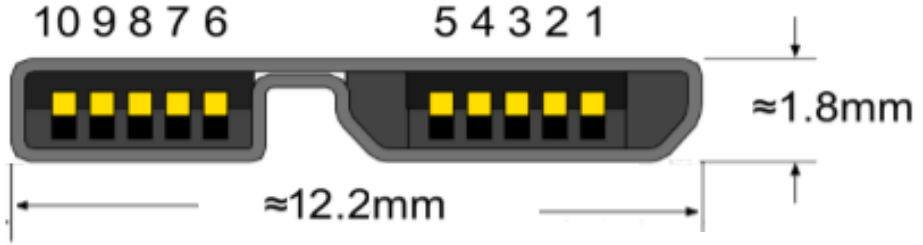
Standard A Plug
(2008)
5Gbps, 5V, 1.8A

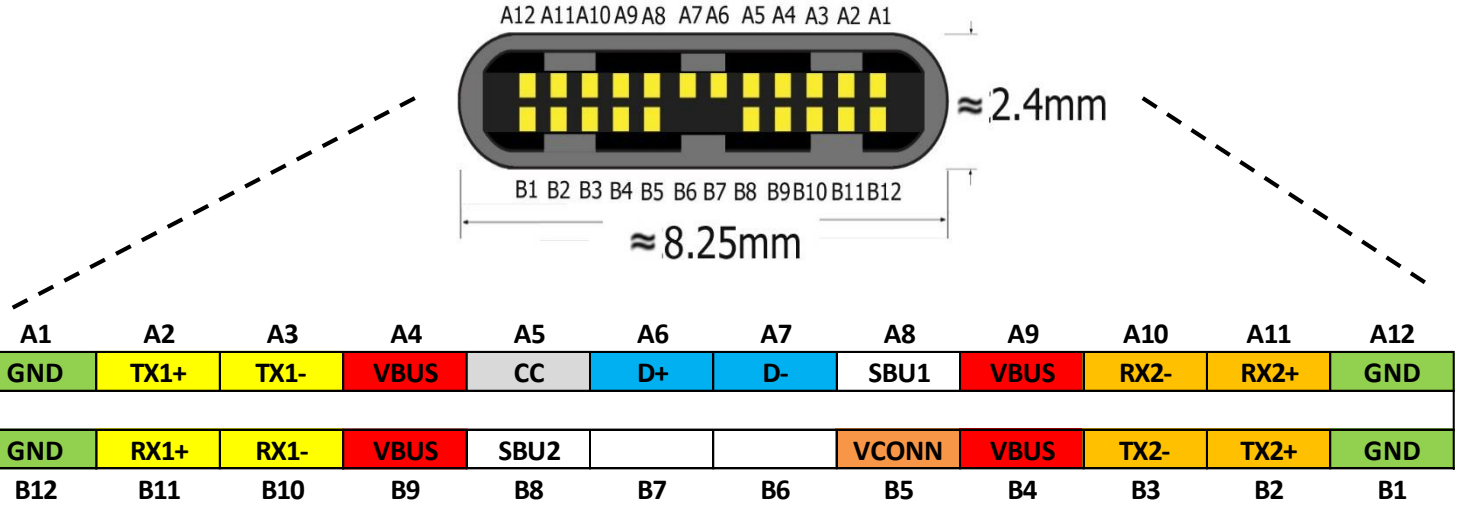
Micro B Plug
(2008)
5Gbps, 5V, 1.8A

USB Type-C Plug
(2014)
10Gbps, 20V, 5A

USB Type-C connector advantage

- Rounded, reversible, flip-able
- ~25% less width vs µ-USB plug
- Signaling and Pins:
  - Two SS differential pairs
  - Vbus power
  - Configuration Channel (CC)
  - USB 2.0 differential pair
  - Sideband Use (SBU)
  - Plug power (Vconn)

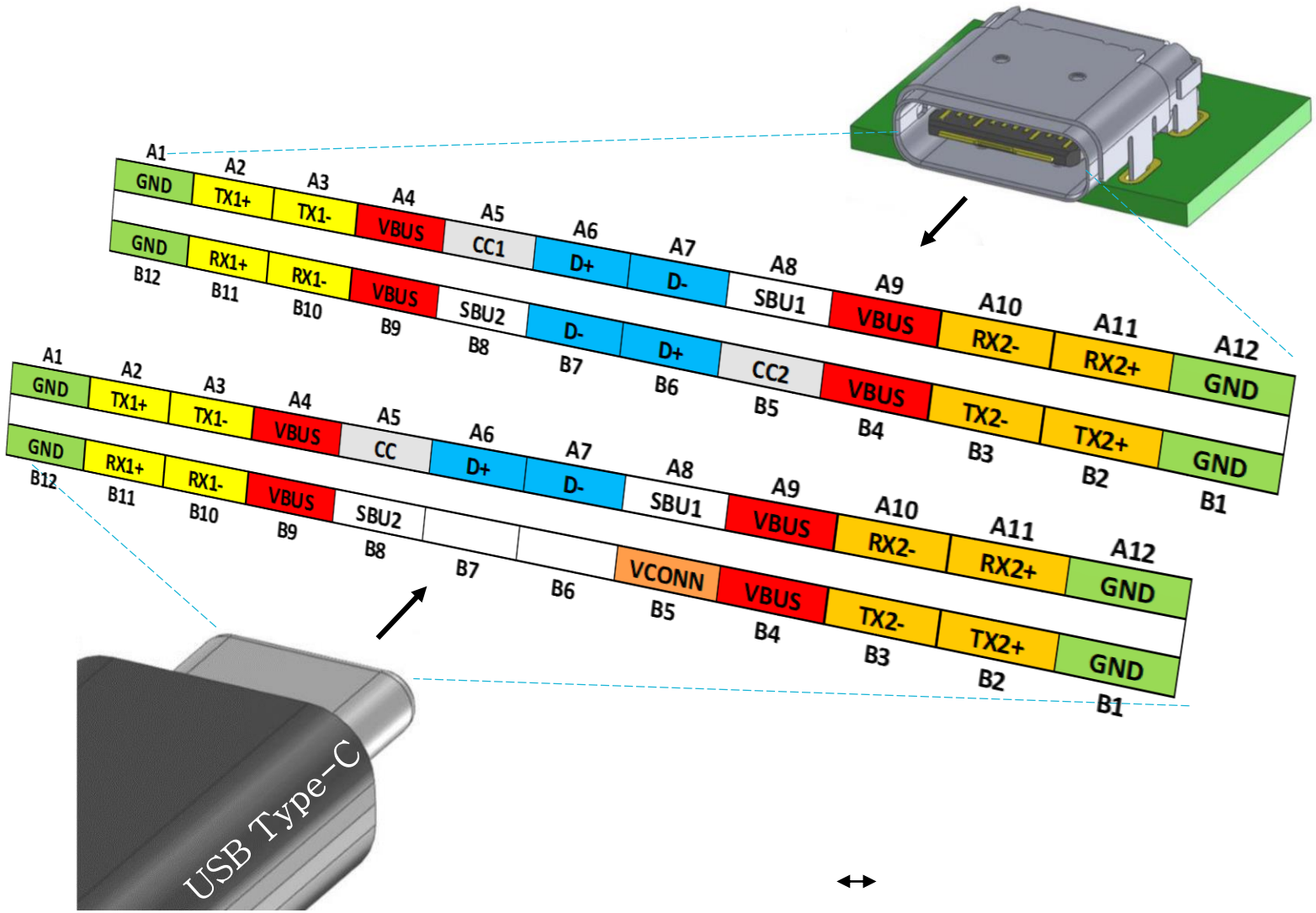




A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2			VCONN	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

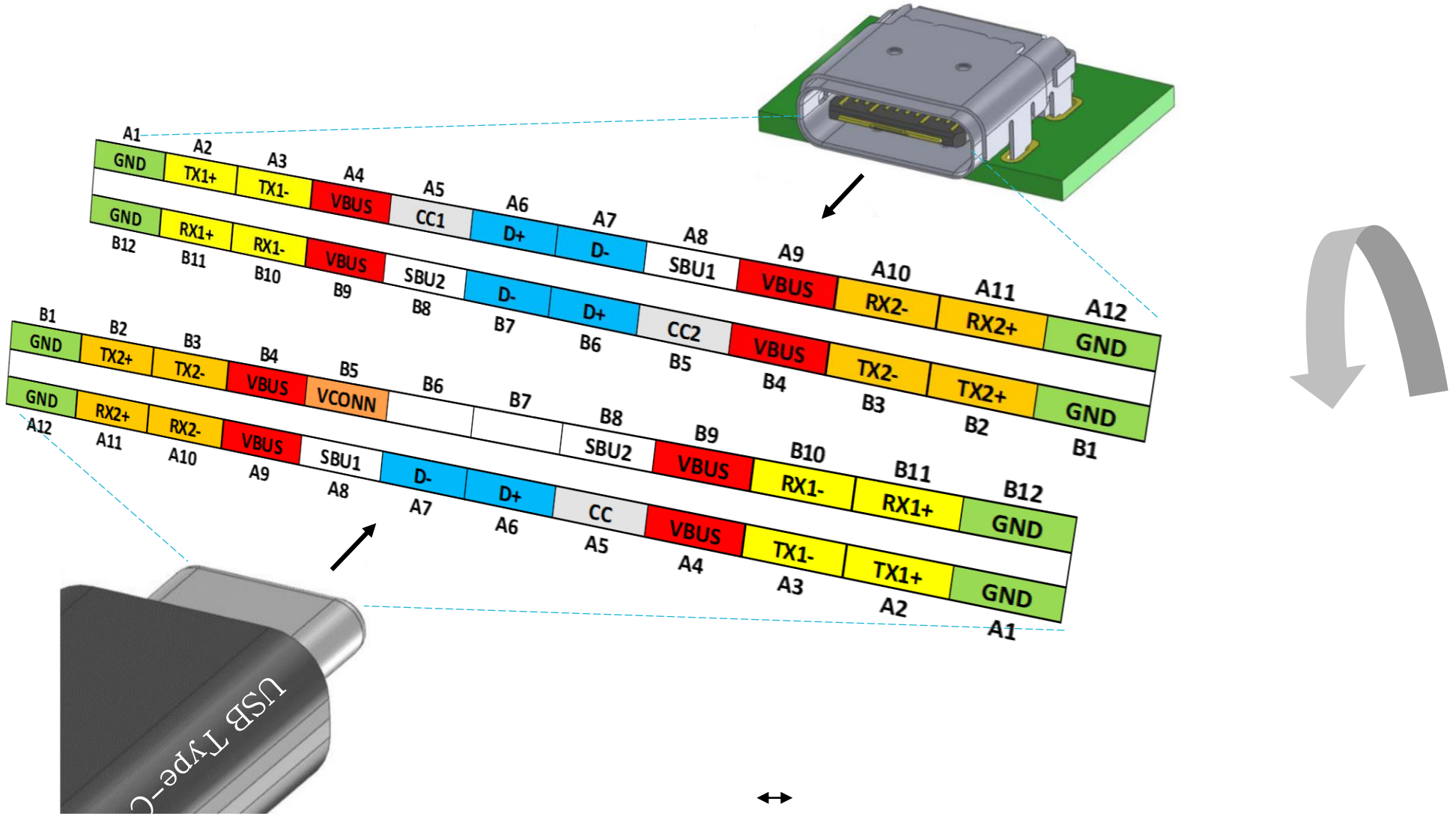
Orientation : Upside Up

“Upside Up”

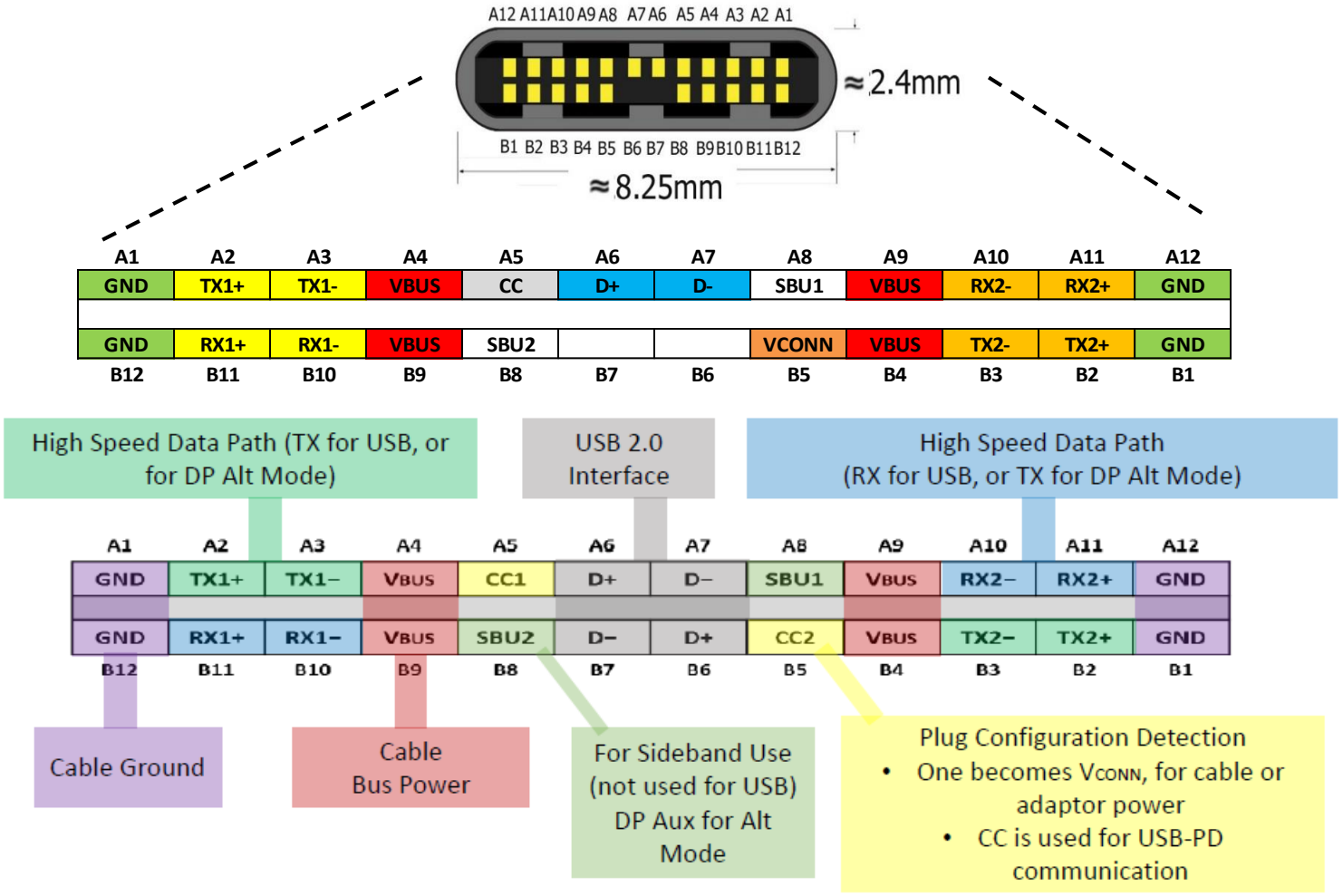


Orientation : Upside Down

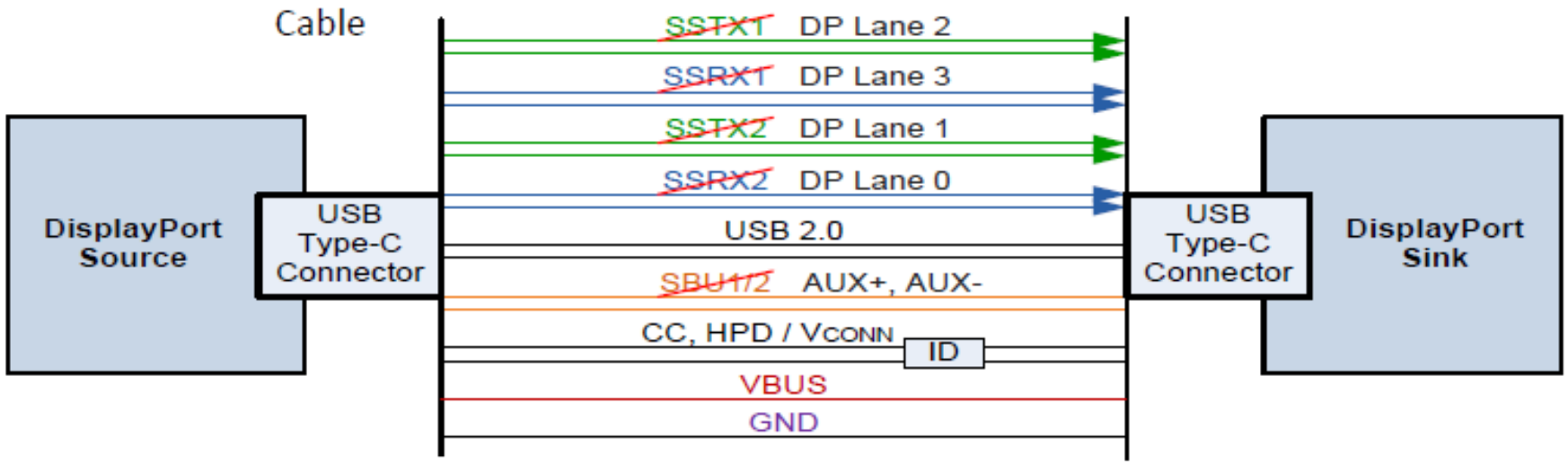
“Upside Down”



USB-C Receptacle pin orientation

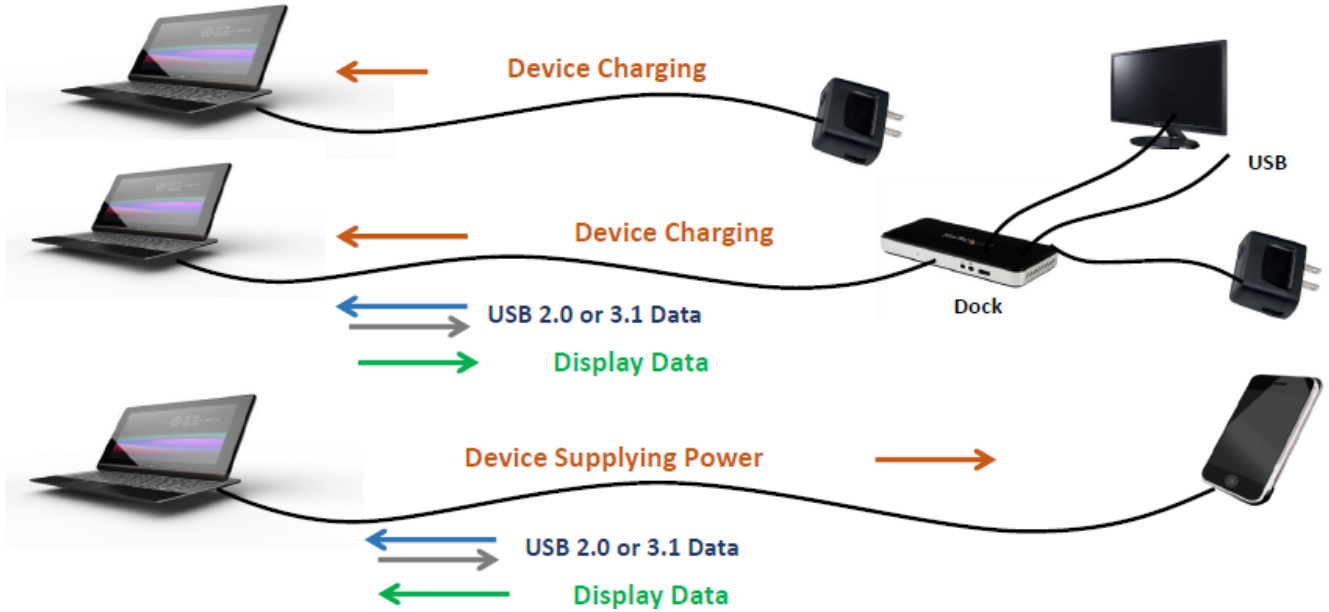


DP over a USB-C to USB-C



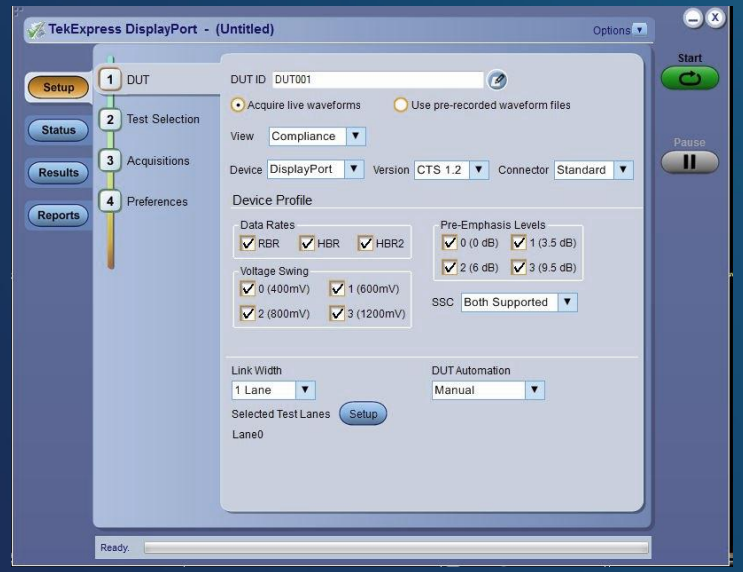
- Utilizes optional DP Alt Mode capability of USB Type-C connector
- DP can use all four high speed lanes to deliver full performance
- The DP AUX Channel uses the SBU pins
- The HPD / IRQ is transmitted over the CC pin using the USB-PD protocol

DisplayPort Alternate Mode on USB Type-C

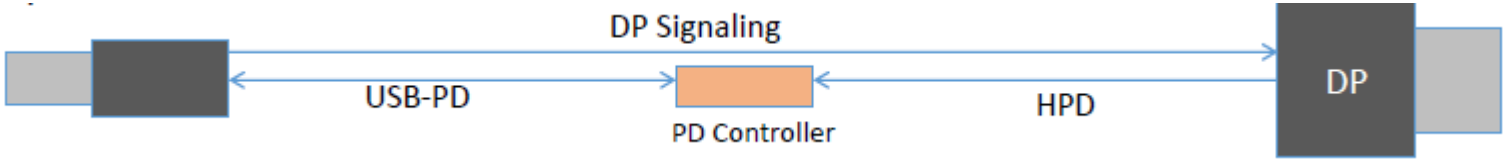


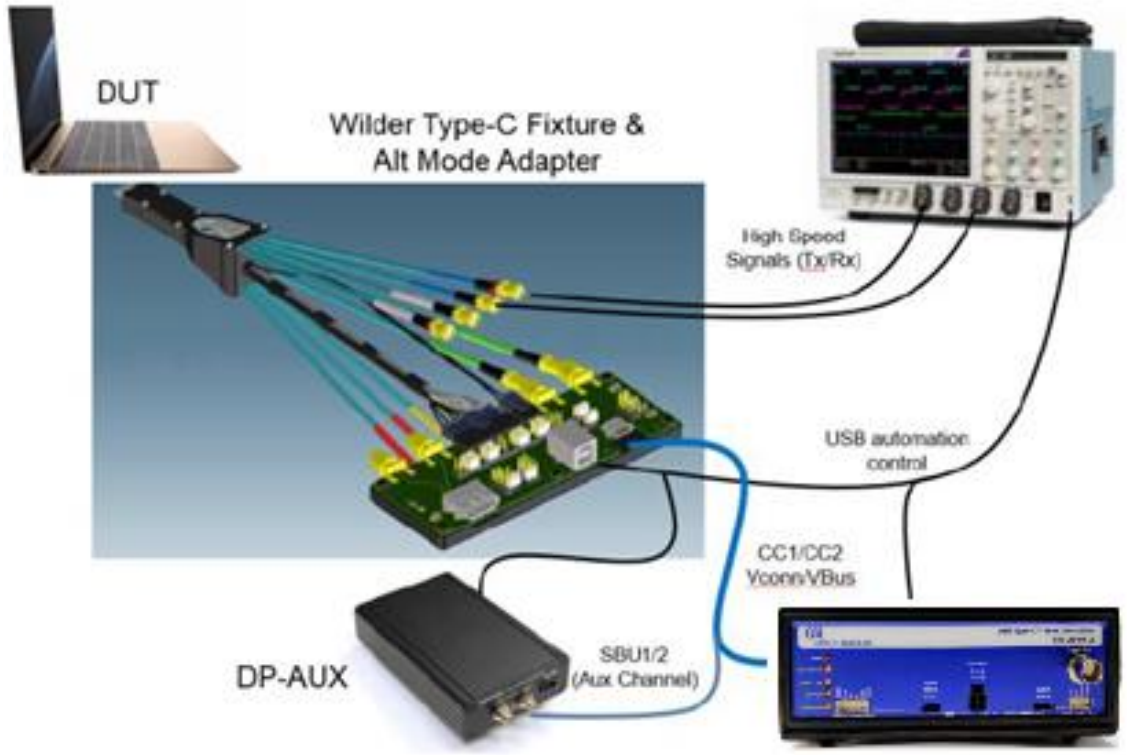
- The VESA DisplayPort Alt Mode Standard, Version 1.0a , was released on Aug 10, 2015
- Enables the use of the USB-C interface for DisplayPort
- Alternate Mode functional extension of the USB-C interface

DP Source Solution



Tektronix DP Type-C configuration



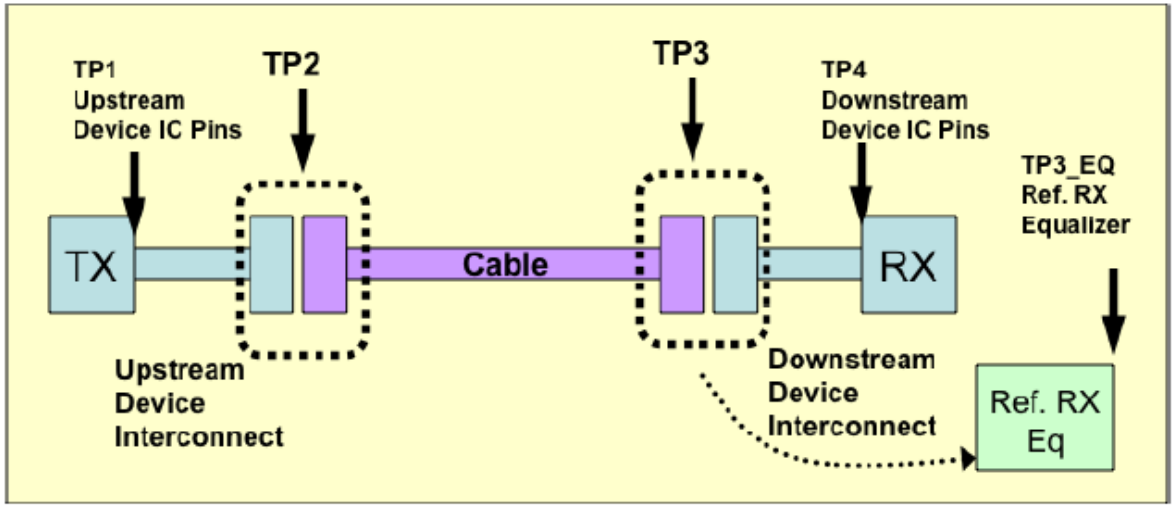


Tektronix Type-C Configuration

Compliance Measurement Points

- TP1: at the pins of the transmitter device
- TP2: at the test interface on a test access fixture near end
- TP3: at the test interface on a test access fixture far end
- TP3_EQ: TP3 with equalizer applied.
- TP4: at the pins of a receiving device

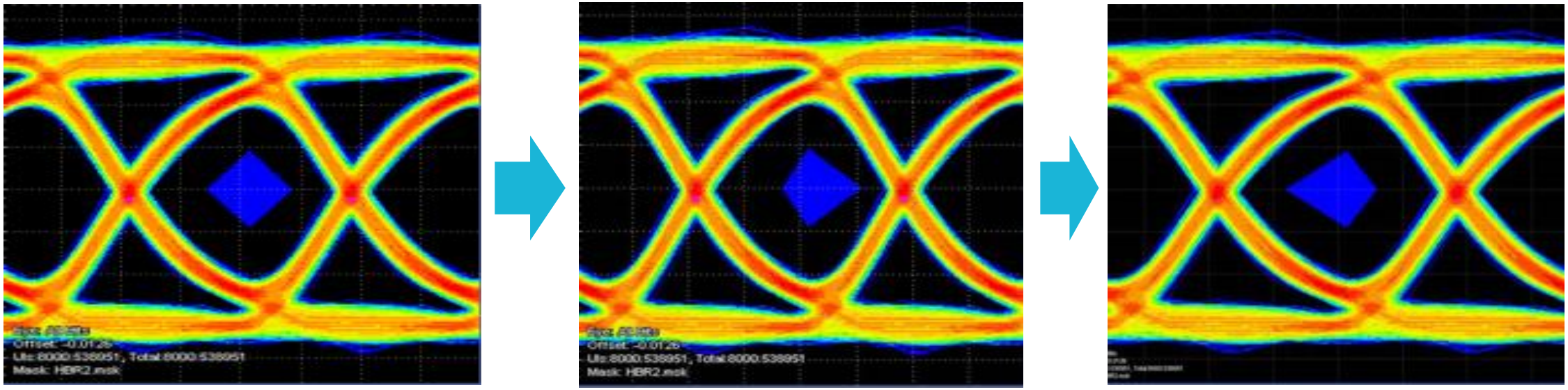
NORMATIVE test points
INFORMATIVE test points



Transmitter Test Overview

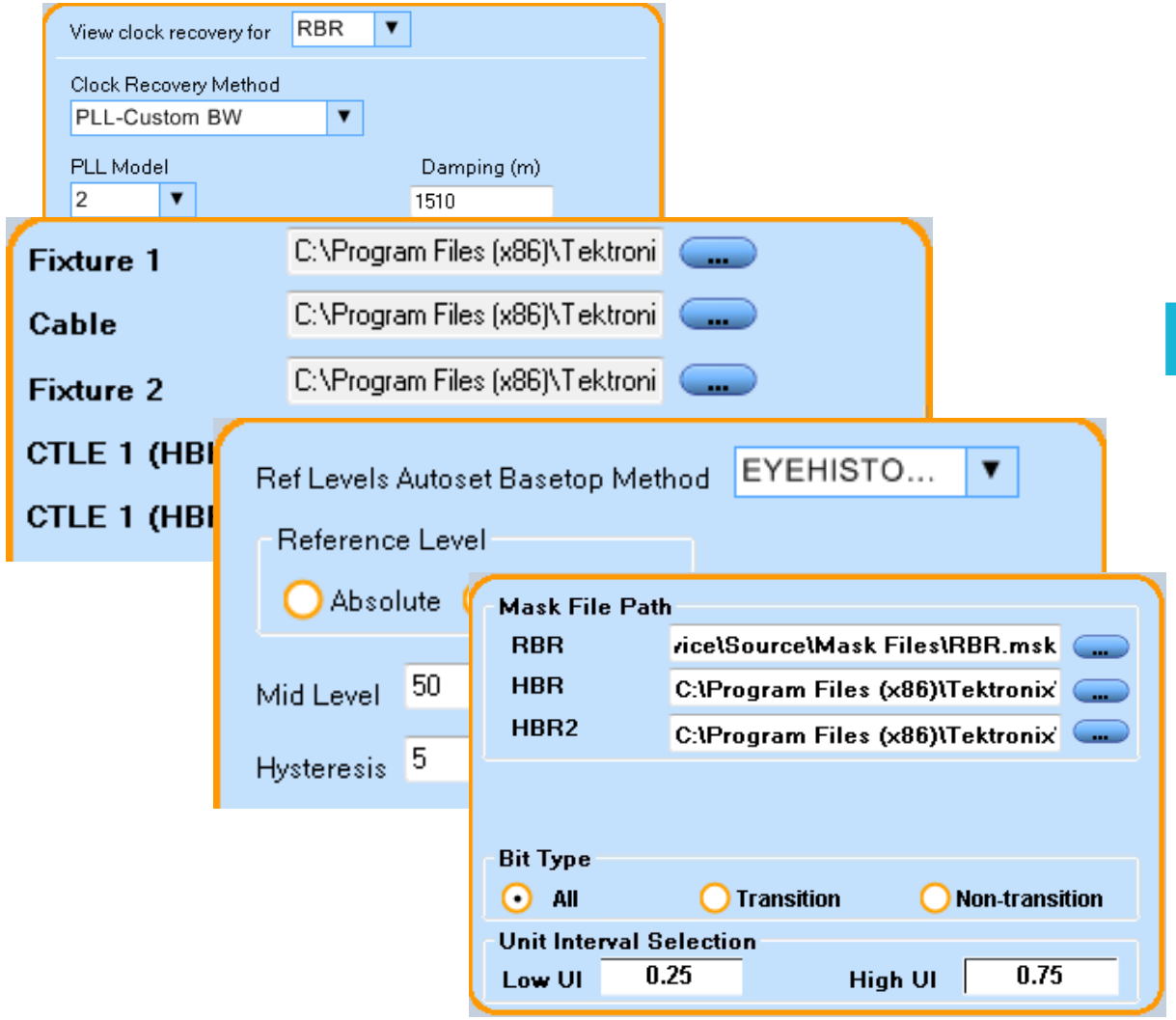
- Standard Tests:
  - Eye Diagram
  - Frequency Accuracy
  - Rise/Fall time
  - Unit Interval
  - TJ/RJ
  - Non ISI Jitter
- Multi-Lane Tests:
  - Inter-pair Skew
  - Intra-pair Skew
- Amplitude Tests:
  - Non Pre-Emphasis Level Verification
  - Pre-Emphasis Level Verification
- SSC Tests:
  - Modulation Frequency
  - Deviation and Variation
- Dual-Mode Tests: (If DUT supports)
  - Clock Jitter &Eye Diagram
- Aux Tests:
  - Sensitivity Test & Eye Diagram

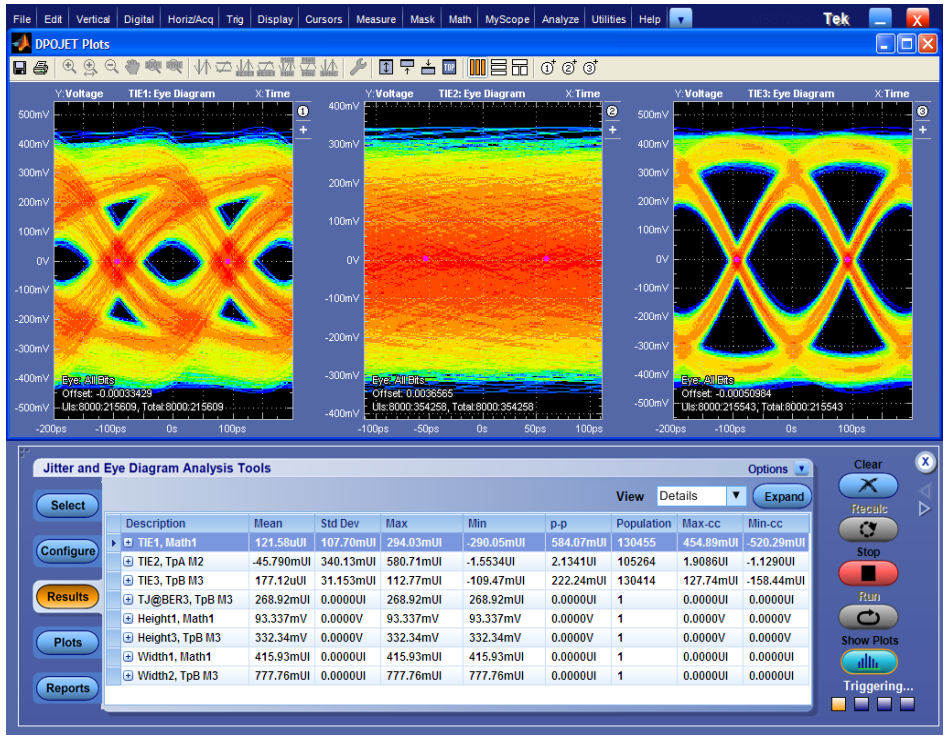
The Eye-diagram



- Adaptive Mask Generation at HBR2 and HBR3
- Width → Along 0mV
- Height → Passing location: 0.375 to 0.625UI
- Eye Diagrams generated for Best case cable (Zero cable) & Worst case cable

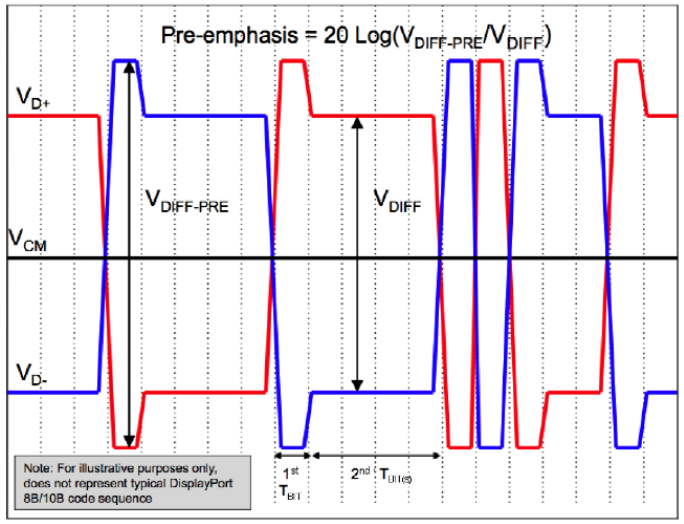
TekExpress Application Advantages





Pre-Emphasis vs Voltage Levels

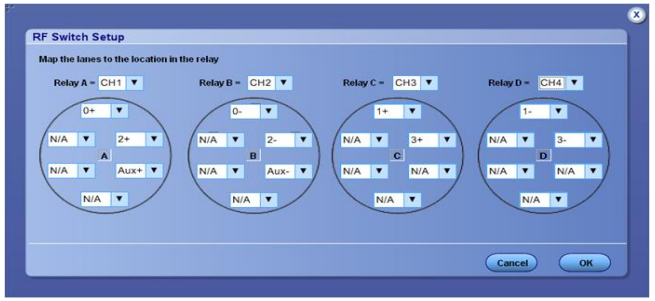
Voltage Swing Level	Pre-emphasis Level			
	Level 0	Level 1	Level 2	Level 3
	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp	Vdiff_pre_pp
0	Required	Required	Required	Optional
1	Required	Required	Required	Not allowed
2	Required	Required	Not allowed	Not allowed
3	Optional	Not allowed	Not allowed	Not allowed



- Non Pre-Emphasis test must measure a region after the signal is settled
- Pre-Emphasis test must measure the region where its being applied
- RBR/HBR – PRBS7 pattern
- HBR2 – PLTPAT (Pre-Emphasis Level Test Pattern)

Measurement Challenges

- Bit Rates: RBR, HBR, HBR2
- Patterns: D10.2,PRBS7, COMP, PLTPAT, PCTPAT
- Pre-Emphasis: 0dB, 3.5dB, 6dB, 9.5dB
- Output Levels: 400mV, 600mV, 800mV, 1200mV
- SSC (Spread Spectrum): On/Off
- Lane Width: 1,2,4



Test	Waveforms (SSC, 4 Lanes Possible Combinations)
Eye Diagram Test	80
Pre-Emphasis Test	240
Non-Pre-Emphasis	32
Total Jitter	80

~432 Acquired signals for DP1.2 Normative Measurements per lane.
X4 lanes results in **1728** Automated acquisitions per DUT

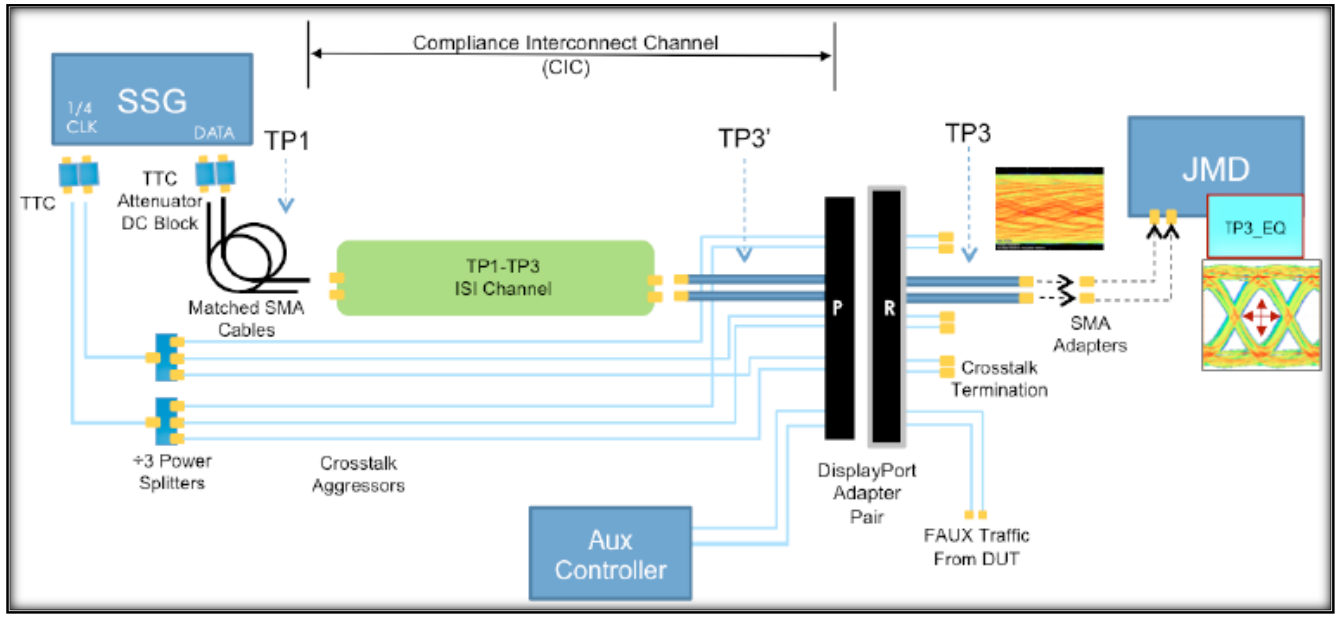
Tektronix DP Solution Configuration/Migration

APPROVED MOI !!!

Std. DP testing		Type-C DP testing (HBR2)
• DPO 70k series with bandwidth >= 12.5GHz	⟷	• DPO 70k series with bandwidth >= 12.5GHz
• 4 x P7313SMA Probes (for Source)	⟷	• 4 x P7313SMA Probes (for Source)
• Option DP12 (TekExpress DP Tx Software)	⟷	• Option DP12 (TekExpress DP Tx Software)
• Option DJA (DPOJET Advanced Jitter Analysis)	⟷	• Option DJA (DPOJET Advanced Jitter Analysis)
• 1 x Aux Controller hardware	⟷	• 1 x Aux Controller hardware
• DP Test fixtures (Available from Wilder in Tek ordering system)	→	• DP Type-C fixtures
	→	• USB Alt-mode controller hardware

DP Sink Solution

Receiver Test Overview - Calibration



- Calibration
  - Frequency Range (SJ): 2MHz, 10MHz, 20MHz, 100MHz
  - Injected Jitter: ISI, RJ and SJ
- TP3 for RBR and TP3_Eq for HBR/HBR2
- BER capability must be supported by Sink chipset

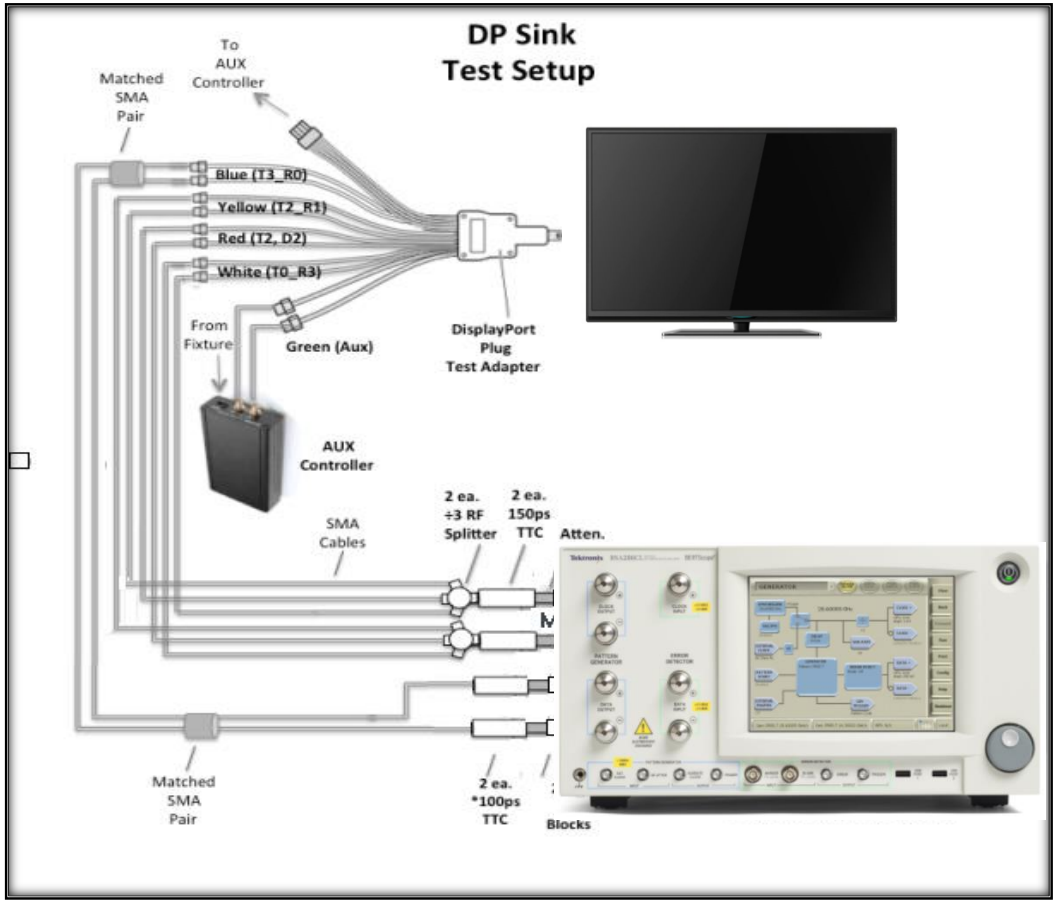
Receiver Test Overview - Compliance

- Perform Link Training
  - Put DUT into test mode
  - Check DUT capabilities
  - Achieve Frequency and Symbol lock
  - Verify BER
- Perform Jitter Tolerance test (Normative)

Table 4-1: Test Parameters for BER Measurement

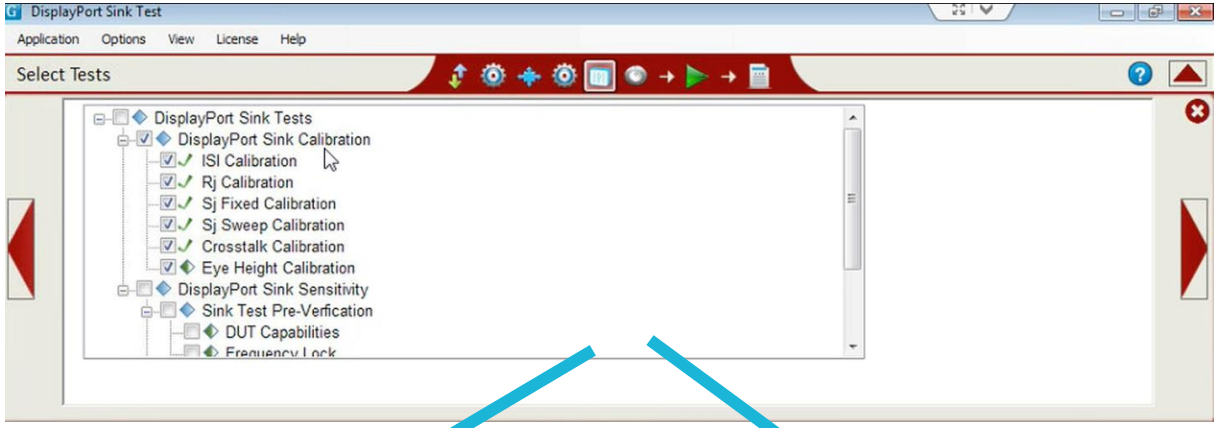
Data Rate	Jitter Frequency	Number of Bits	Max Number of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR2 HBR RBR	2MHz	10^{12}	1000	HBR2 = 185s HBR= 370s RBR= 620s	0
HBR2 HBR RBR	10MHz	10^{11}	100	HBR2= 19s HBR= 37s RBR= 62s	+350ppm +350ppm +350ppm
HBR2 HBR RBR	20MHz	10^{11}	100	HBR2= 19s HBR= 37s RBR= 62s	0
HBR2 HBR	100MHz	10^{11}	100	HBR2= 19s HBR= 37s	0

*To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds*

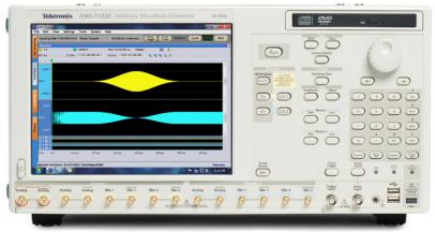


DisplayPort Sink Test SW – GRL-DP-SINK

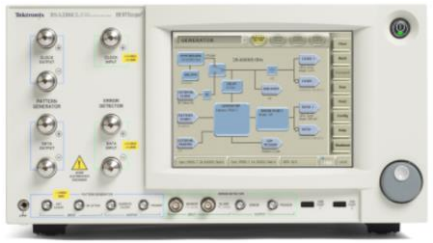
- Controller in Charge for Oscilloscope and BERT for Calibration Stage
- Industry Leading Calibration Times:
  - HBR2
  - HBR
  - RBR
  - Total < 1 Hr.
- All with the same setup!



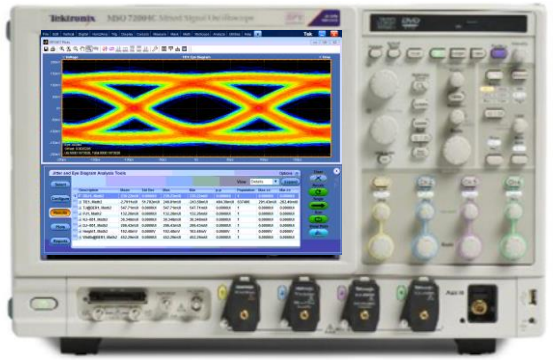
Your Choice Of Generator!



AWG

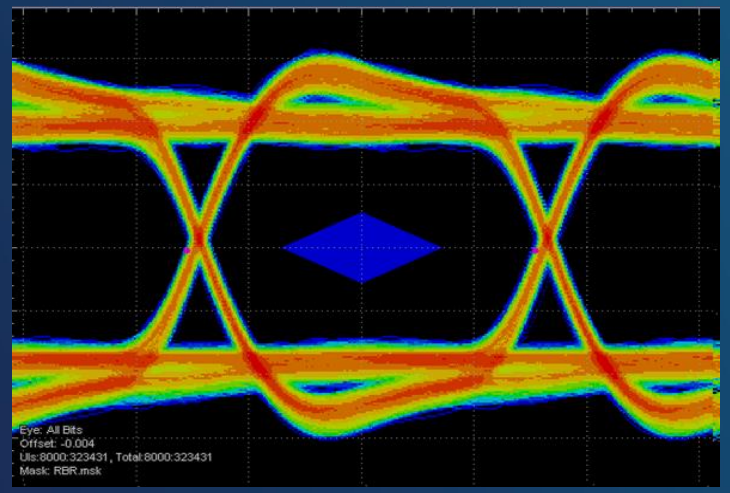


BERTScope
(Recommended)



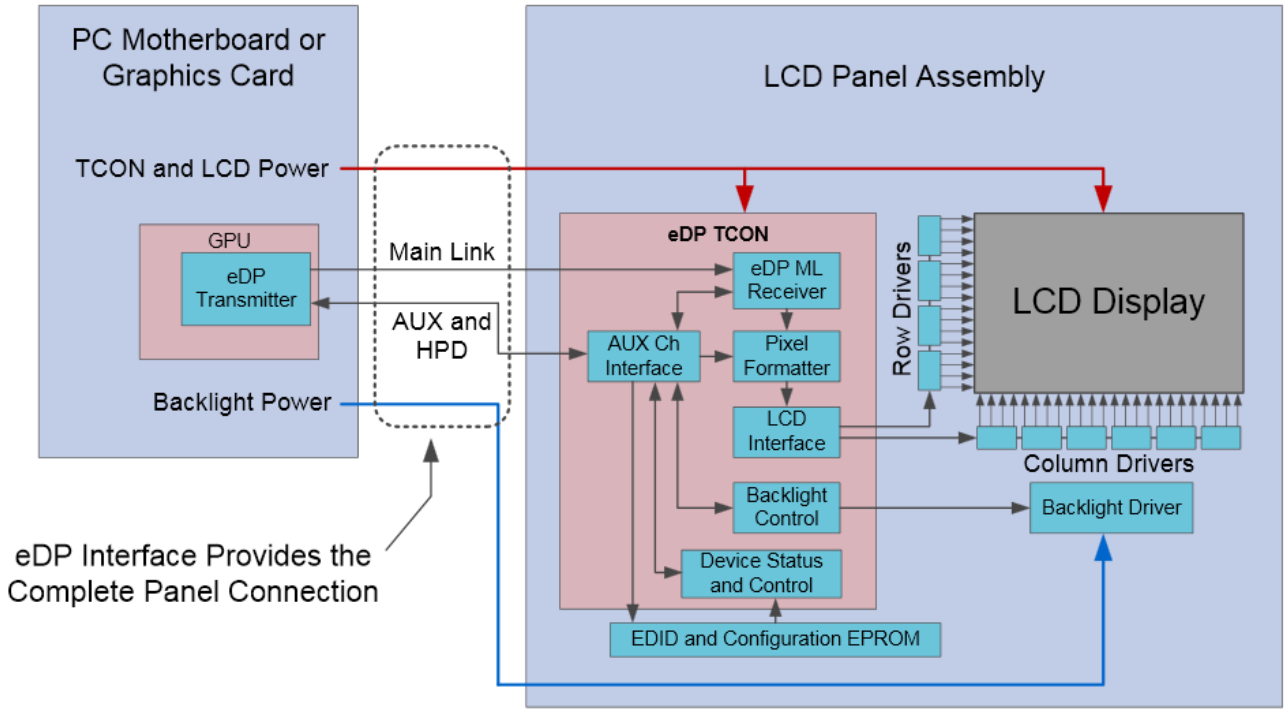
TekScope

eDP Source Solution



eDP 1.4 Basics

- eDP Source → Integrated into the video/graphics processor circuit, such as in the GPU of a notebook PC
- eDP Sink → Integrated into the display processor, such as in the LCD timing controller (TCON) of a notebook PC
- eDP Cable → A 20 to 50-pin connector will be used for multi-lane implementations

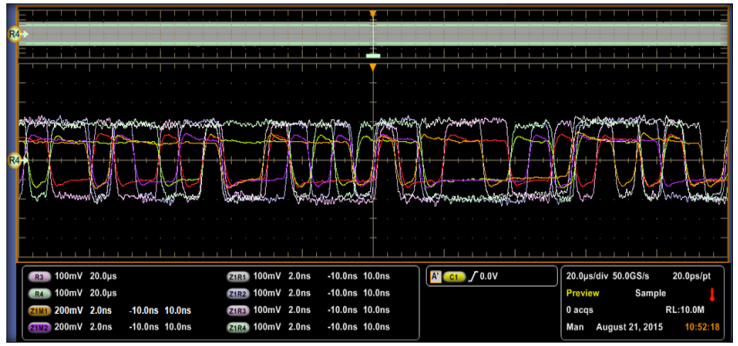


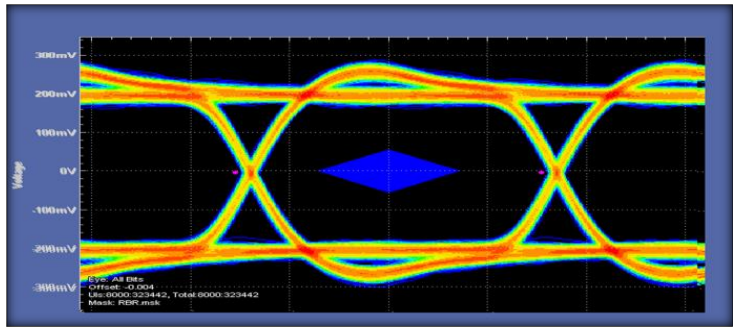
Measurements Challenges

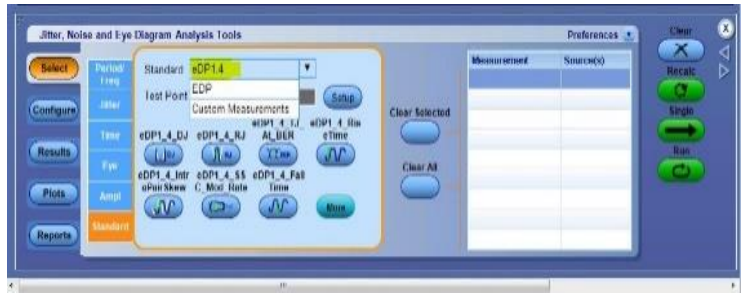
- Probing
  - Need to probe TP3 (pins of the Tx device)
  - Wilder breakout fixture interfaces with motherboard
  - During measurement CTLE is applied to measure the TP3_EQ point
- Eye-diagram
  - Mask is created dynamically based on the signal characteristics for all speeds
  - Auto-mask fit optimally places mask during measurement
- SSC measurements
  - SSC helps to keep EMI low. If DUT supports SSC, need to test with SSC ON and OFF.
- Intermediate data rates
  - Unlike RBR,HBR and HBR2, eDP supports intermediate data rates
    - RBR, **R216, R243**, HBR, **R324, R432**, HBR2
  - System needs to be tested for all of the intermediate data rate increasing test time

Option EDP14 : Key Features

- Compliant to the latest eDP standard
- DPOJET based application; easy to recall setup files
- Support for one, two or four lane test configuration
- Generates dynamic mask for Eye diagram tests based on the configuration and signal levels
- Detailed DPOJET reports with screenshots and waveform info



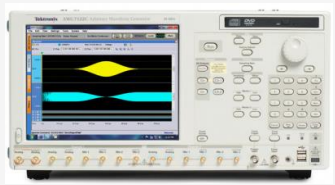




Tektronix DisplayPort Solutions

Signal Generation

AWG 7k/70k series



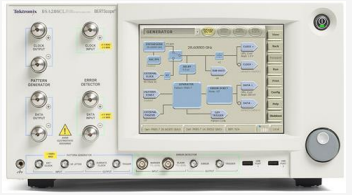
Device Under Test
ASIC/FPGA, transceivers, physical layer ICs

Signal Acquisition

DPO70000DX series
Real Time Oscilloscope

DPO70000SX ATI NEW!
Real Time Oscilloscope

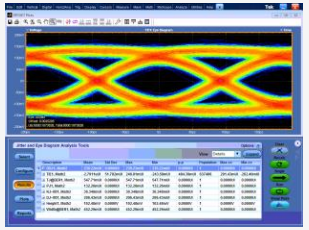
BERTScope



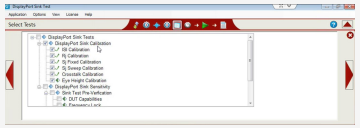
Analysis Software

TekExpress
Compliance Analysis SW

DPOJET RT Jitter & Timing Analysis



Receiver Compliance Software

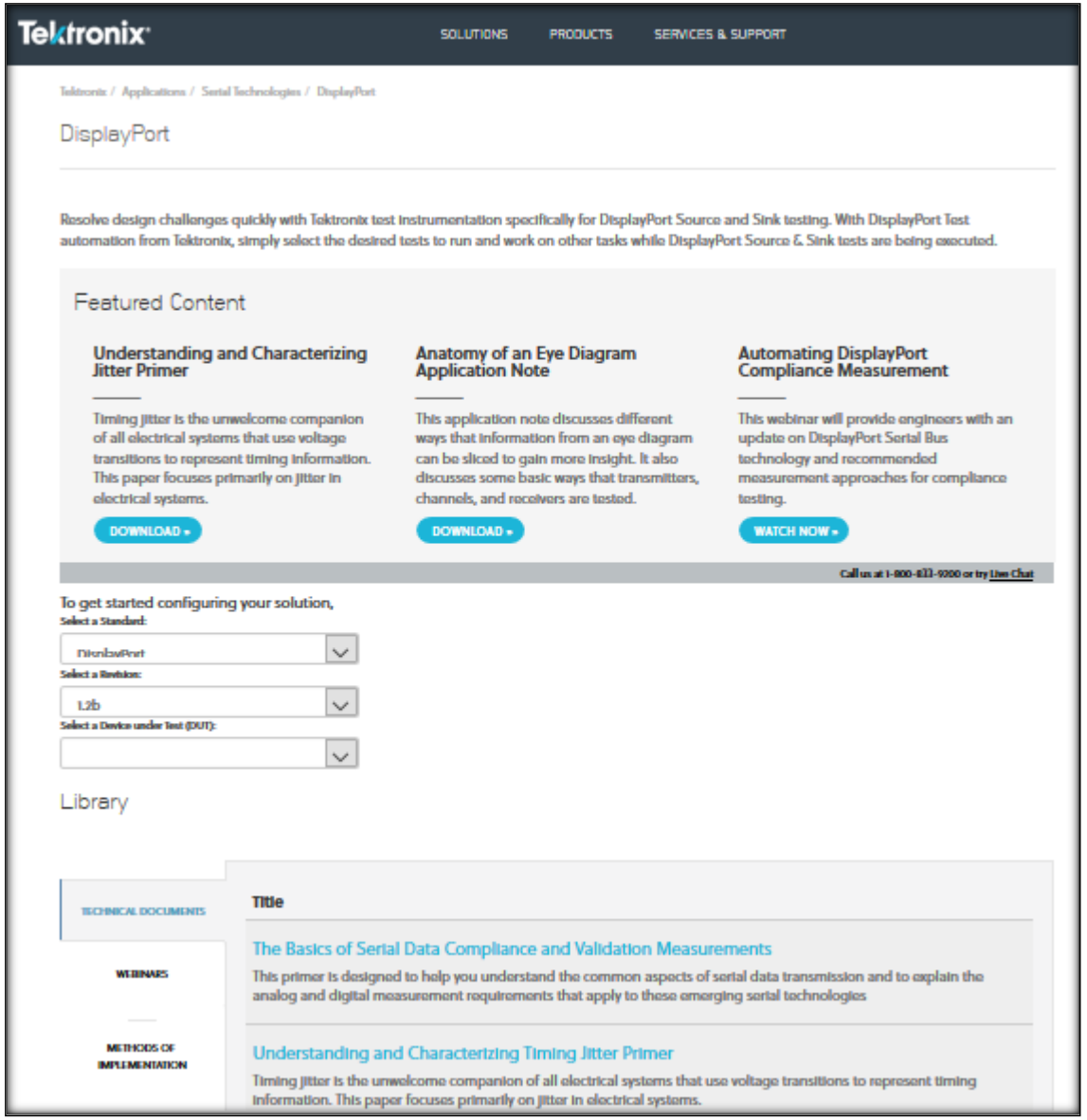


Summary of key Advantages

- Automation → Faster test times, ease of use
- Switching support → Hands free testing with RF switch
- Approved → Use the solution with confidence
- Ease of use → Caters both Compliance & Characterization users
- Flexibility → Modify the parameters according to testing needs
- Migration → Easy from Standard DP to Type-C

Information for DP

- http://www.tek.com/displayport-0
- Webinars
- Application Notes
- Methods of Implementation
- Product & Software Datasheets
- Software Download Trials

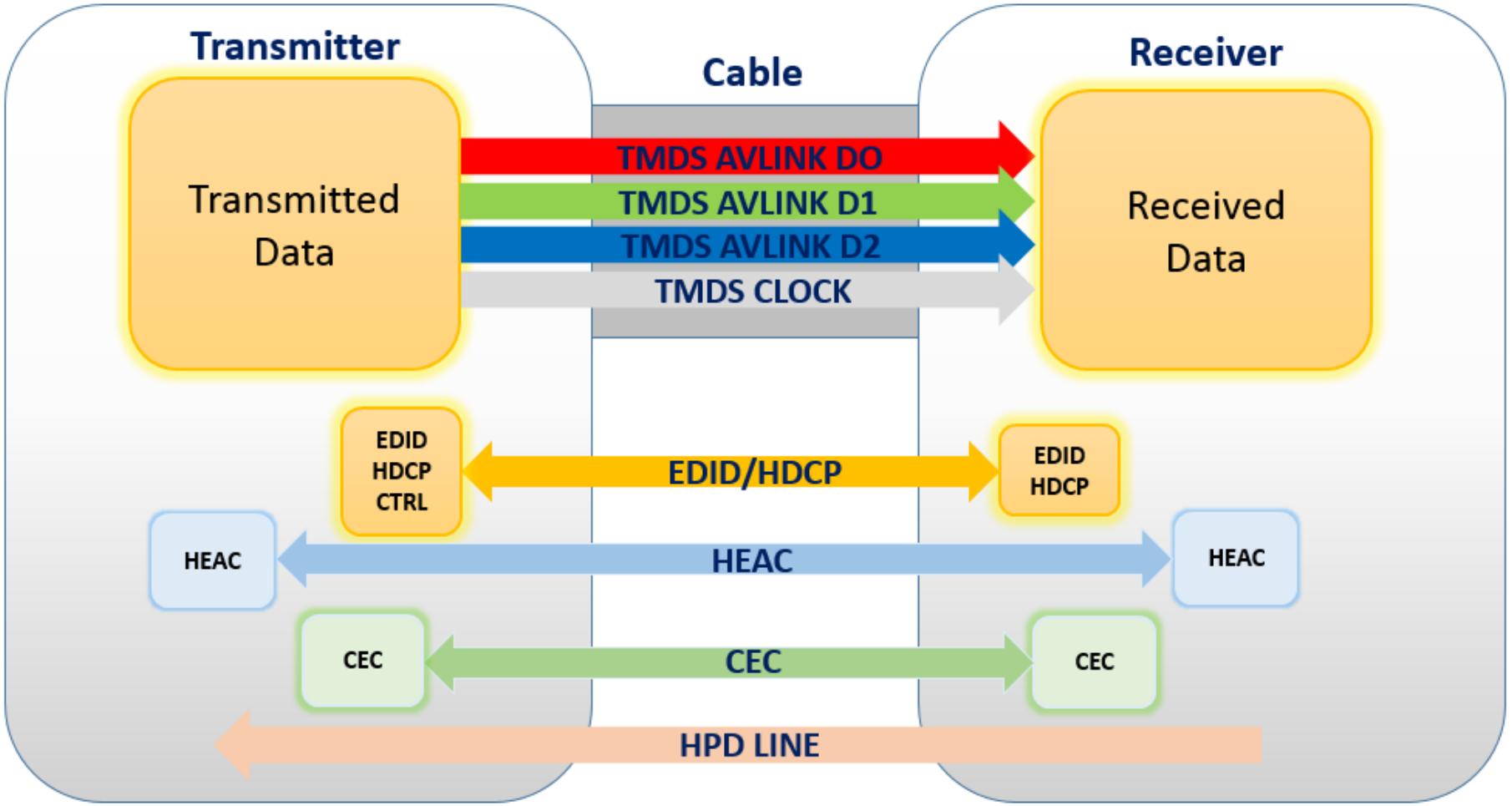


HDMI

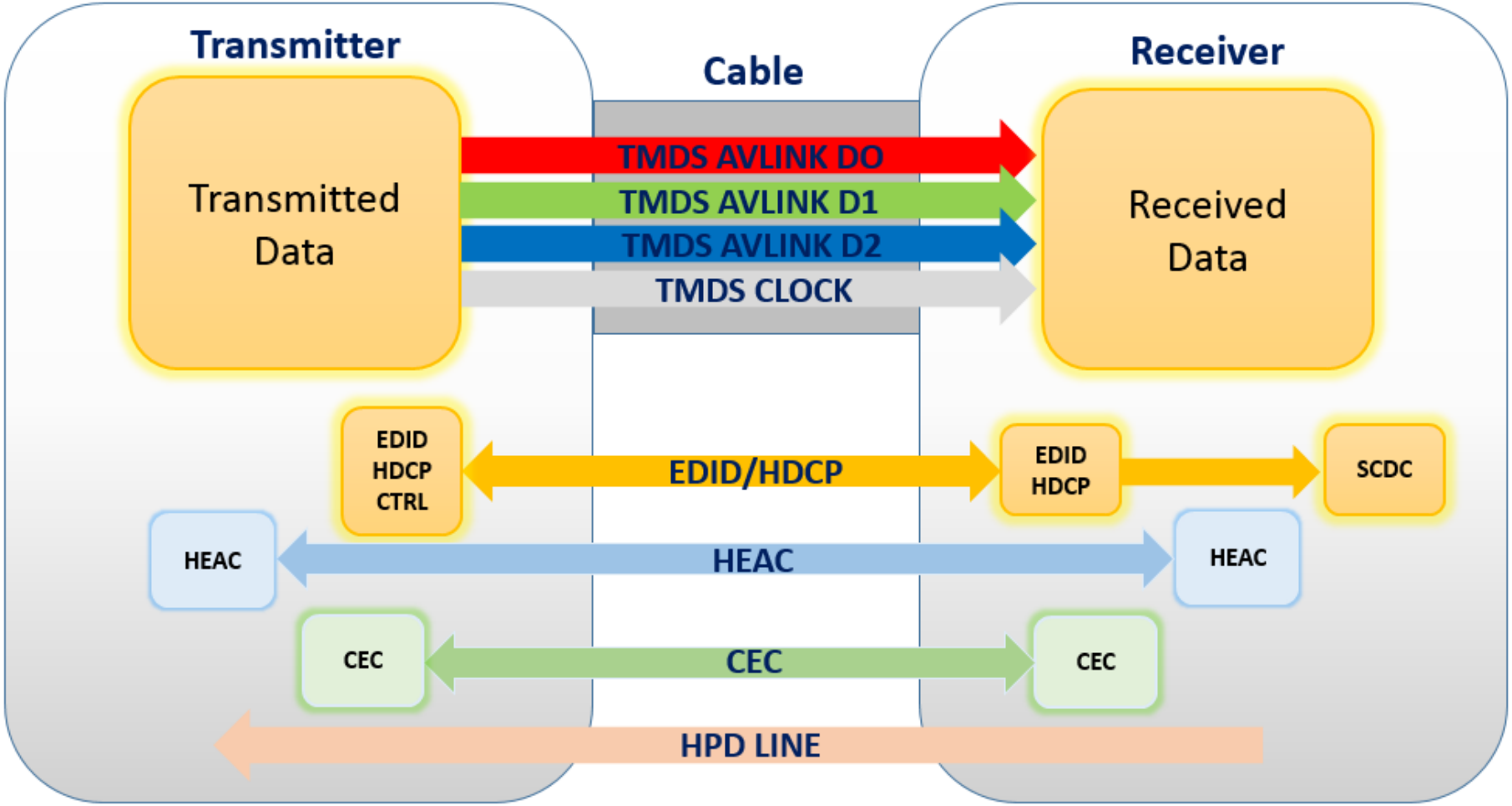
HDMI Evolution

HDMI Version	1.0	1.1	1.2	1.3	1.4	2.0
Release Dates	12/09/2002	5/20/2004	8/22/2005	6/22/2006	6/09/2009	9/4/2013
Max. Bandwidth	4.95	4.95	4.95	10.2	10.2	18
Max. Pixel clock rate	165	165	165	3.4	3.4	6
Max. Resolution	1600x1200p60	1600x1200p60	1600x1200p60	2048x1536p75	4096x2160p24	4096x2160p60
Audio Channels	8	8	8	8	8	32
Max Audio Sampling Rate	768kHz	768kHz	768kHz	768kHz	768kHz	1536kHz

HDMI 1.4 Architecture



HDMI 2.0 Architecture



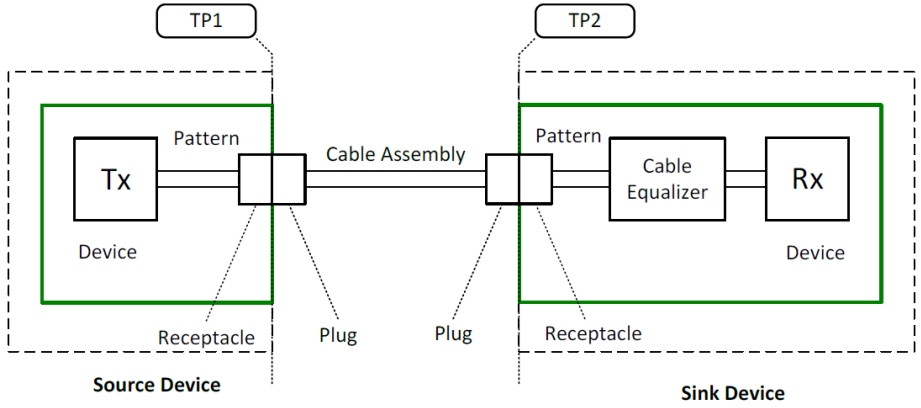
Source Testing differences

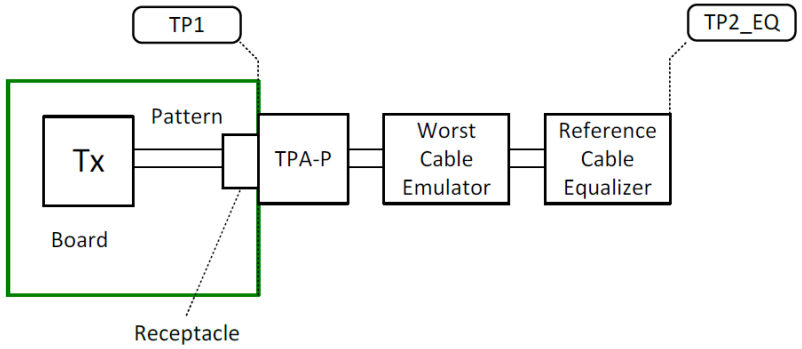
HDMI 1.4			HDMI 2.0		
Test ID	Test point	Test Mode	Test ID	Test point	Test Mode
7-2 TMDS VL	TP1	Single-ended	HF1-1 VL and Vswing	TP1	Single-ended
7-4 TMDS Rise and Fall Times		Differential	HF1-2 Rise and Fall times	TP1	Differential
7-6 TMDS Inter pair skew		Differential	HF1-3 Inter pair skew	TP1	Differential
7-7 TMDS Intra-pair skew		Single-ended	HF1-4 Intra-pair skew	TP1	Single-ended
7-8 TMDS Clock Duty cycle		Differential	HF1-6 Clock Duty cycle	TP1	Differential
7-9 TMDS Clock Jitter		Differential	HF1-7 Clock Jitter	**TP2_EQ**	Differential
7-10 TMDS Data Eye diagram		Differential	HF1-8 Data Eye Diagram	**TP2_EQ**	Single-ended
7-3 Voff		Single-ended	**HF1-5 Differential Voltage**	TP1	Differential

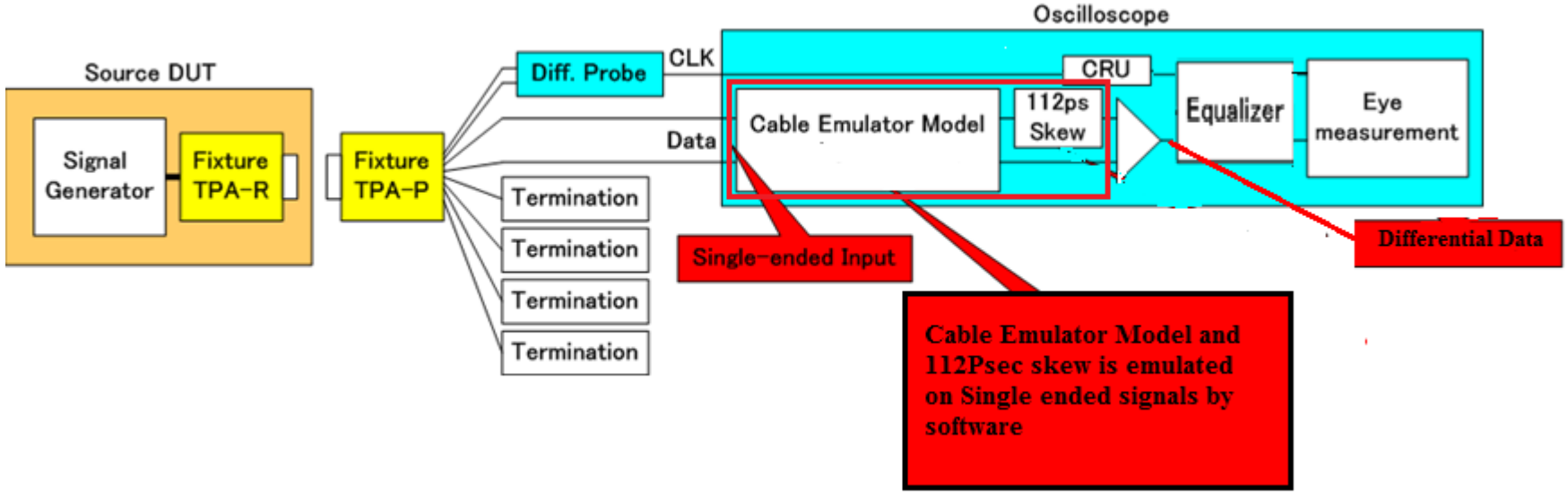
Source Testing Requirements

- CTS 1.4b tests is a pre-requisite for HDMI 2.0
- Min Scope BW required from 8 GHz to 16GHz
  - Highest data rate increased from 3.4GHz to 6Ghz
- New set of fixtures
- New software Options
  - Option HDM for HDMI 2.0, Option HT3 for HDMI 1.4

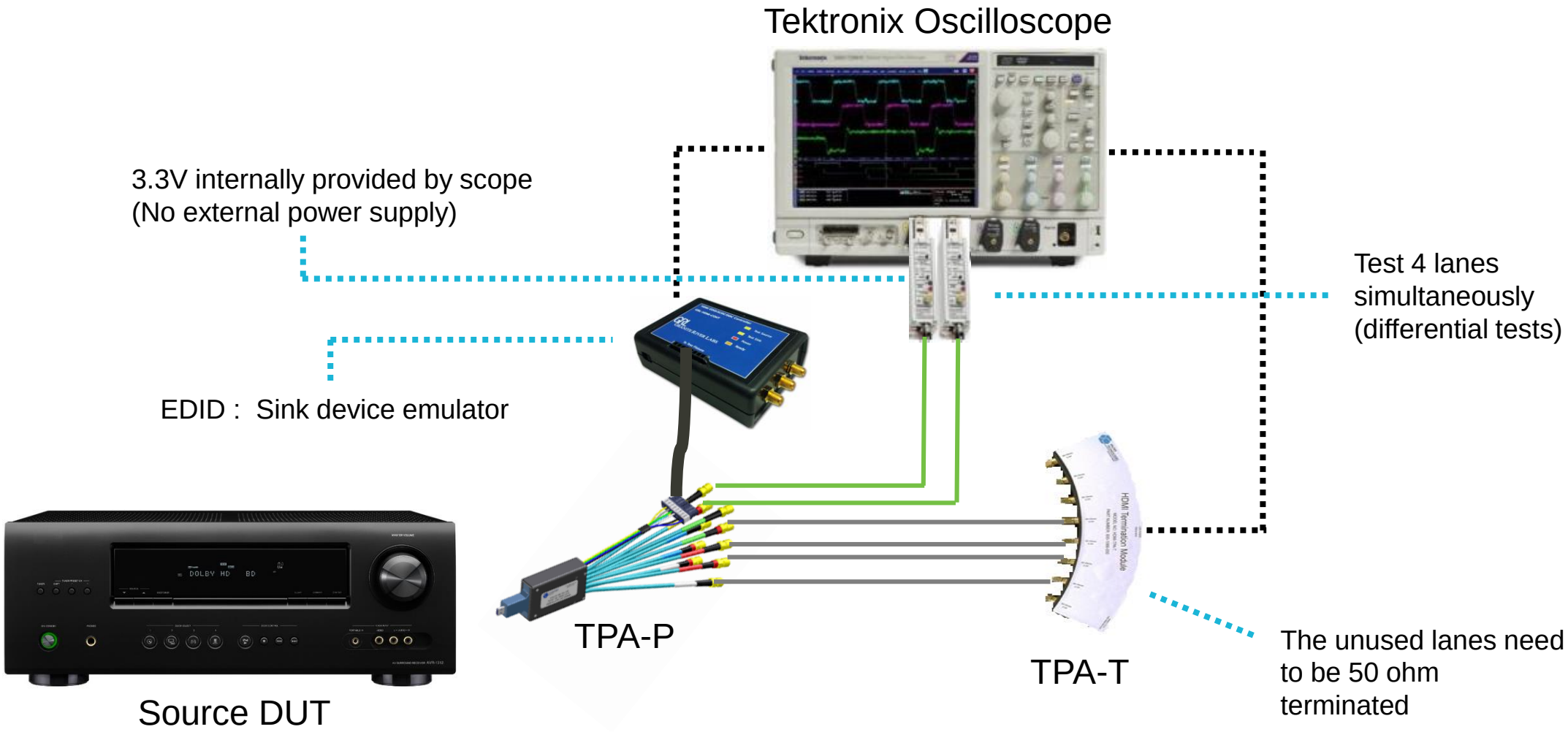
HDMI test points







Source Test Setup overview



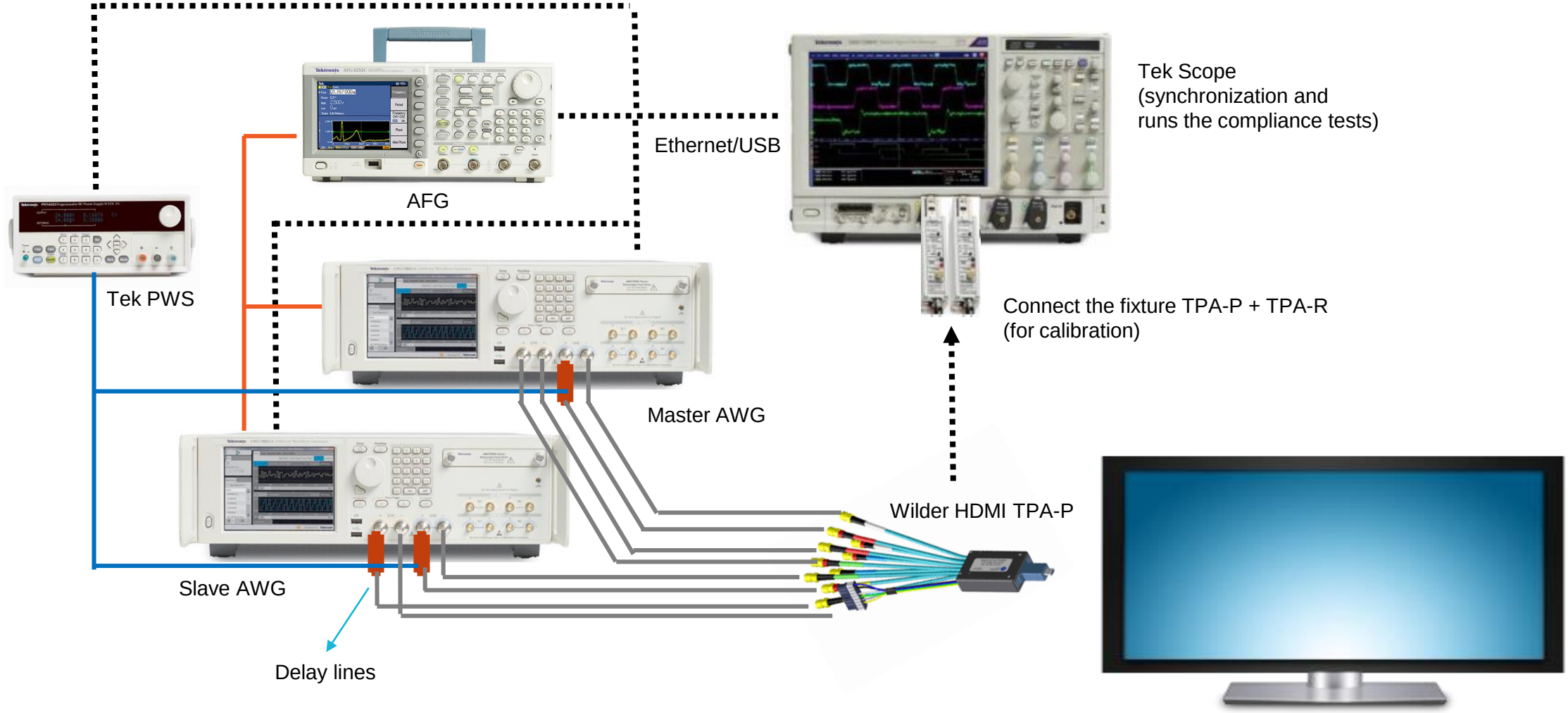
HDMI 2.0 Source Equipment List

- DPO/MSO 70k series Oscilloscope with BW >= 16GHz
- DPOJET Advanced Jitter Analysis (Opt DJA)
- TekExpress HDM software (Opt HDM)
  - Opt HT3 (TDSHT3 for 1.4 testing) is pre-requisite
- HDMI 2.0 Fixture set (can be used for HDMI 1.4b testing)
- 3 x P7313SMA differential probes (4 x recommended)
- 1 x EDID Emulator
  - Order from GRL p/n GRL-HDMI-CONT

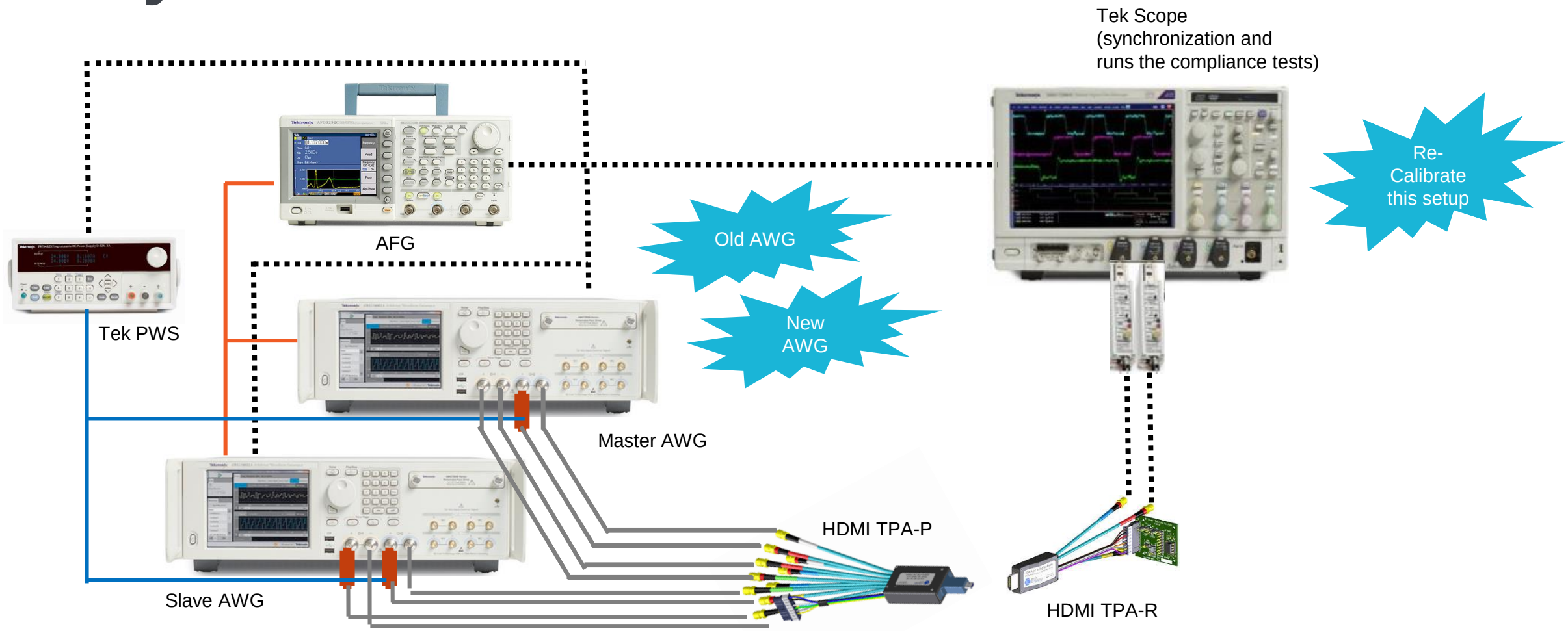
Sink Testing Requirements

- Sink Jitter Tolerance test needs fixed 112ps ***hardware*** delay line
- Sink Intra-pair skew test needs to be skewed with variable ***hardware*** delay lines
- New set of fixtures
- HDMI 1.4b testing is a pre-requisite for HDMI 2.0

HDMI 2.0 Sink Test setup

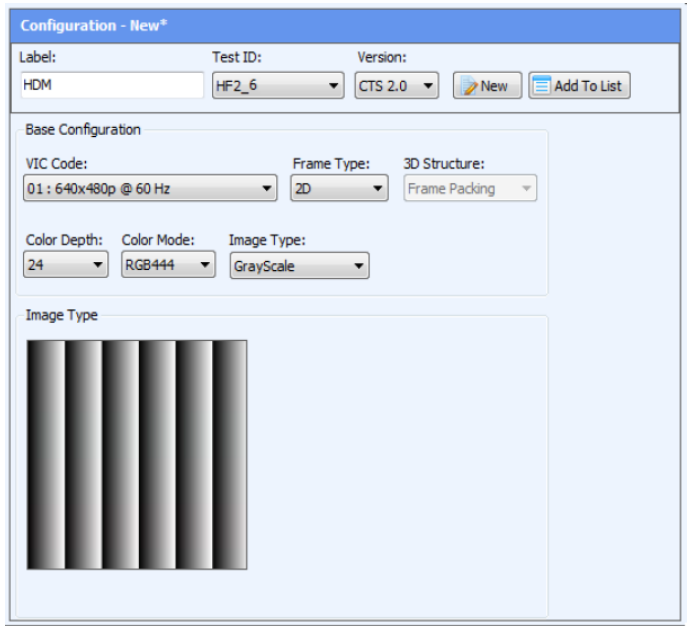


Why is Calibration needed?



HDMXpress Software

- Automate HDMI 2.0/1.4 pattern creation
- Batch process → create multiple patterns at a time
- Supports:
  - VIC specified CEA861-F specification
  - Color depths : 24bit, 30bit, 36bit, 48bit
  - 3D frame types
  - Aspect ratio tests
  - Images : Gray scale, Color Bar, Chess board, Custom image
  - Color Sub-samplings : RGB, YCBCR 4-4-4, YCBCR 4-2-0, YCBCR 4-2-2
- Supports Closed Loop calibration
  - Calibrates Voltage Swing and Jitter at TP2 and FP1/FP2



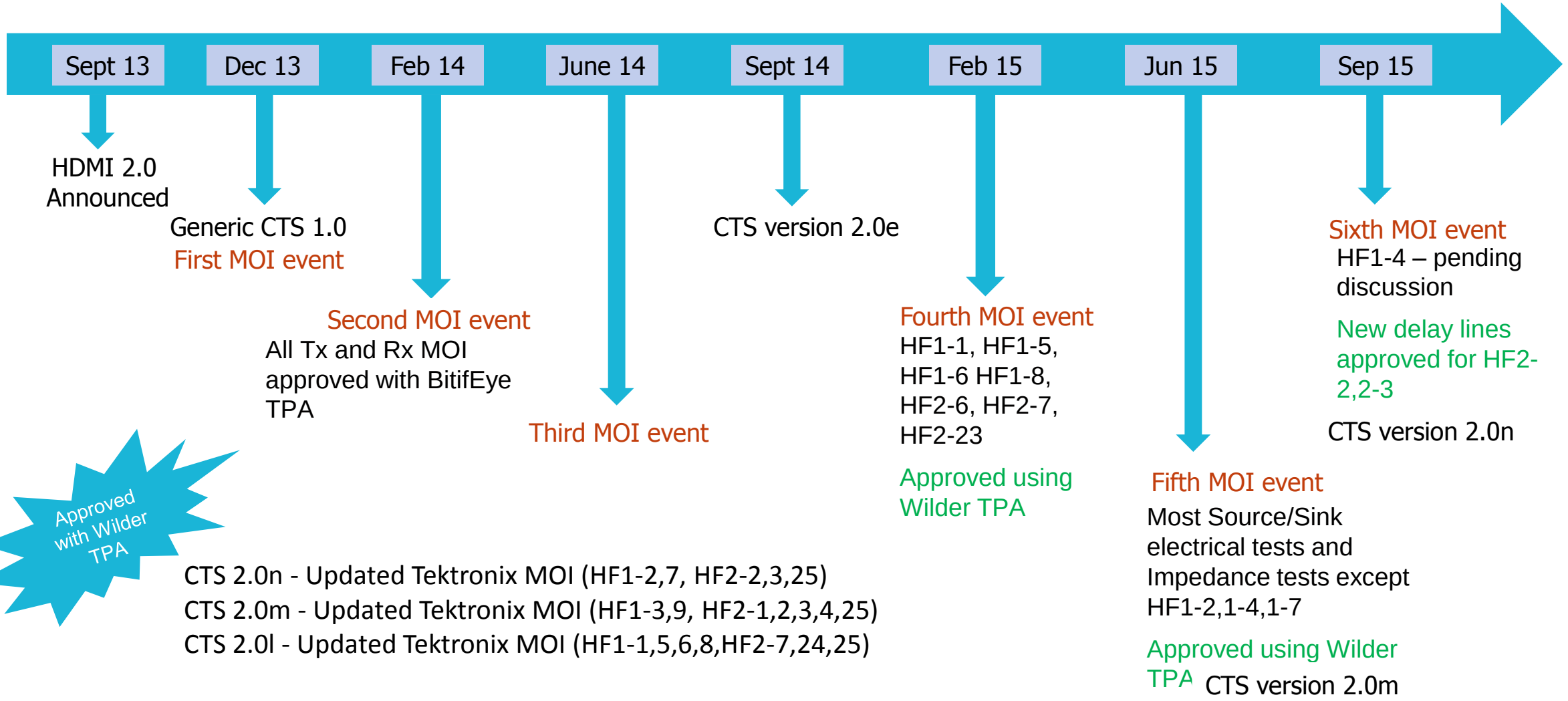
HDMI 2.0 Sink Equipment List

- DPO 70k series Oscilloscope with BW >= 16GHz
- Option HDM-DS/HT3-DS
- Option HDM-DSM (for Calibration and pattern creation)
- HDMI 2.0 Fixture set
- 3 x P7313SMA differential probes (Eye-diagram verification)
- 2 x AWG70002A (with Option 01, 225 and 03-sequencing)
- 1 x AFG 3102C for synchronization
- HDMI DS-Accessories kit

HDMI 2.0 Sink Equipment List

- 6 x Delay line for introducing fixed 112 ps skew from Spectrum
  - Each delay line gives 56ps of delay
  - p/n : 8001-SM21-02
- 1 x Variable delay line from Spectrum for adjusting skew
  - p/n : LS-0170-1121
- 1 x Programmable Dual Channel Power supply
  - PWS4205/PWS4305 or equivalent
- 1 x I2C Analyzer
  - Order from GRL p/n : GRL-HDMI-CONT

MOI Events – Approval status



Tektronix HDMI Solutions

Signal Generation

AWG 70k series

Device Under Test
ASIC/FPGA, transceivers, physical layer ICs

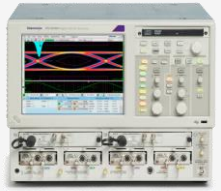
Signal Acquisition

DPO70000DX series
Real Time Oscilloscope

DPO70000SX ATI
Real Time Oscilloscope

NEW!

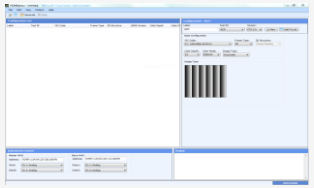
Sampling Scope
Impedance measurement



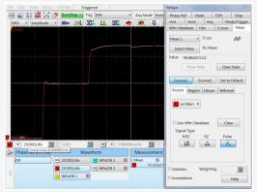
Analysis Software

TekExpress
Compliance Analysis SW

HDMXpress
Calibration tool



Automated Impedance measurement tool



Tektronix Serial Standards Body Participation

John Calvin

Pavel Zivny

Rob Marsland

Oliver Kiehl

Anshuman Bhat

Gary Simonton

UN Vasudev

Tim Bieber

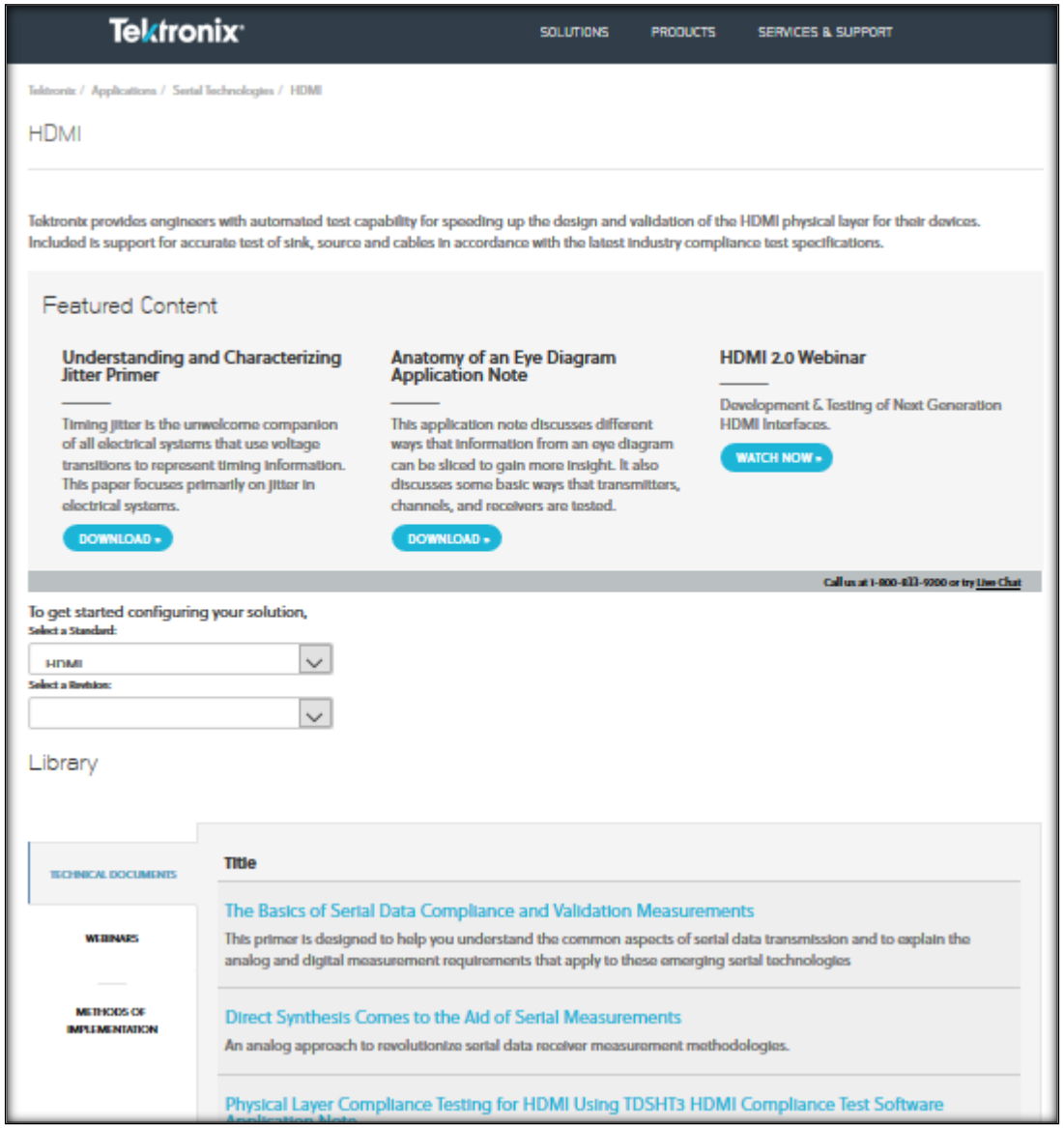
Kalev Sepp, PhD

Keyur Diwan

Yogesh Pai

Information for HDMI

- http://www.tek.com/hdmi-0
- Webinars
- Application Notes
- Methods of Implementation
- Product & Software Datasheets
- Software Download Trials



Thanks!