Tektronix

Memory Interface Electrical Validation LPDDR4

3/14/2016

Anshuman Bhat – Product Line Marketing Manager
Oliver Kiehl – Principle Engineer

Agenda

- DRAM Standard Basic – LPDDR4
- Signal Acquisition and Analysis – LPDDRx
- Questions

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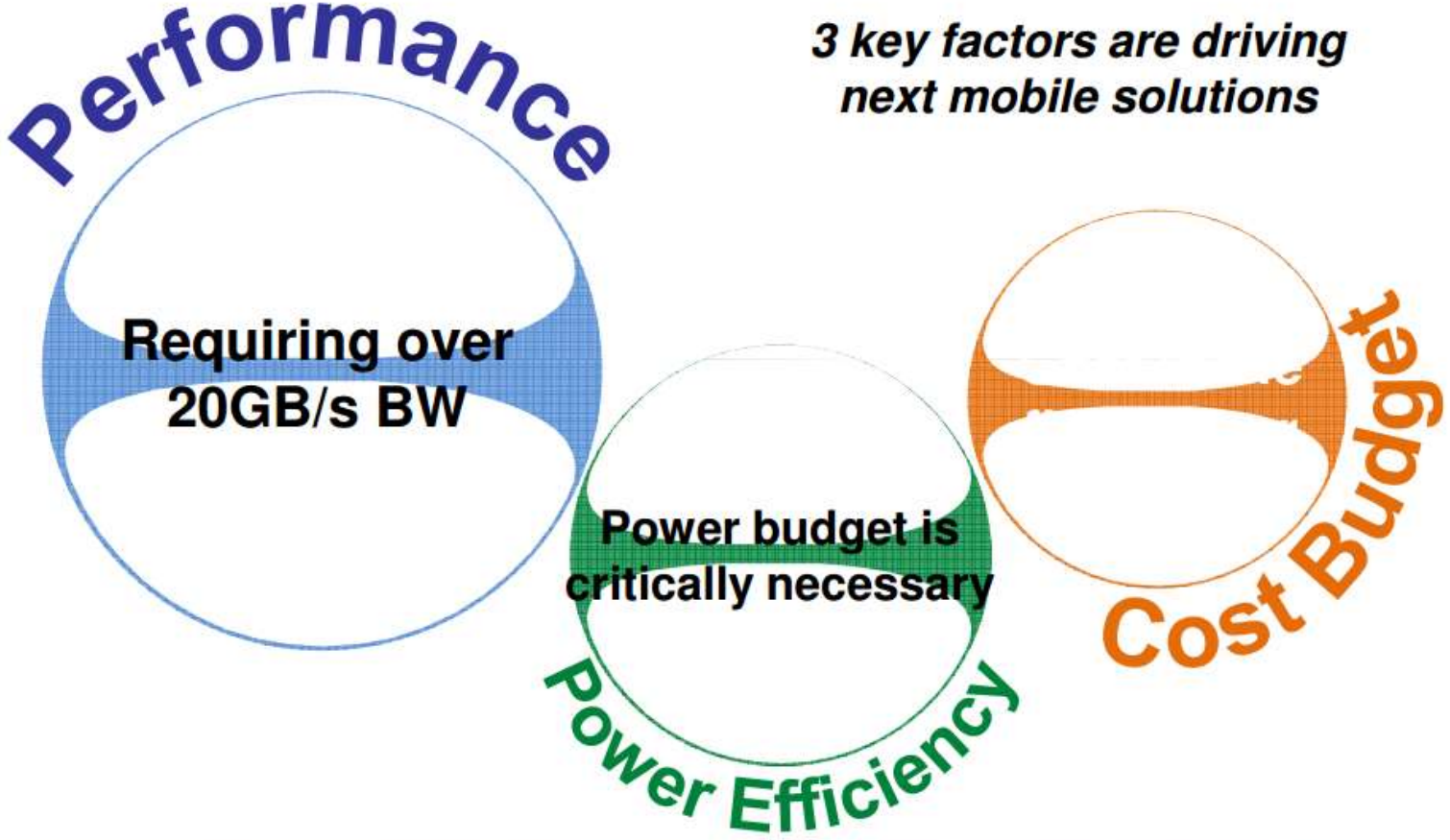
DRAM Standard Basic – LPDDR4

3/14/2016

Section Agenda

- DRAM Standard Basic – LPDDR4
  - Motivation
  - Overview (LPDDR3 – LPDDR4 Comparison)
  - Architecture
  - Pin Comparison
  - Training/Calibration
  - Parameter Definition
    - Vcent
    - Mask Parameters
    - tDIPW, VIHL_AC
  - Read Write Timing
  - VSSQ Referenced Signaling
  - Beyond LPDDR4

Key Factors Driving Mobile Eco-System

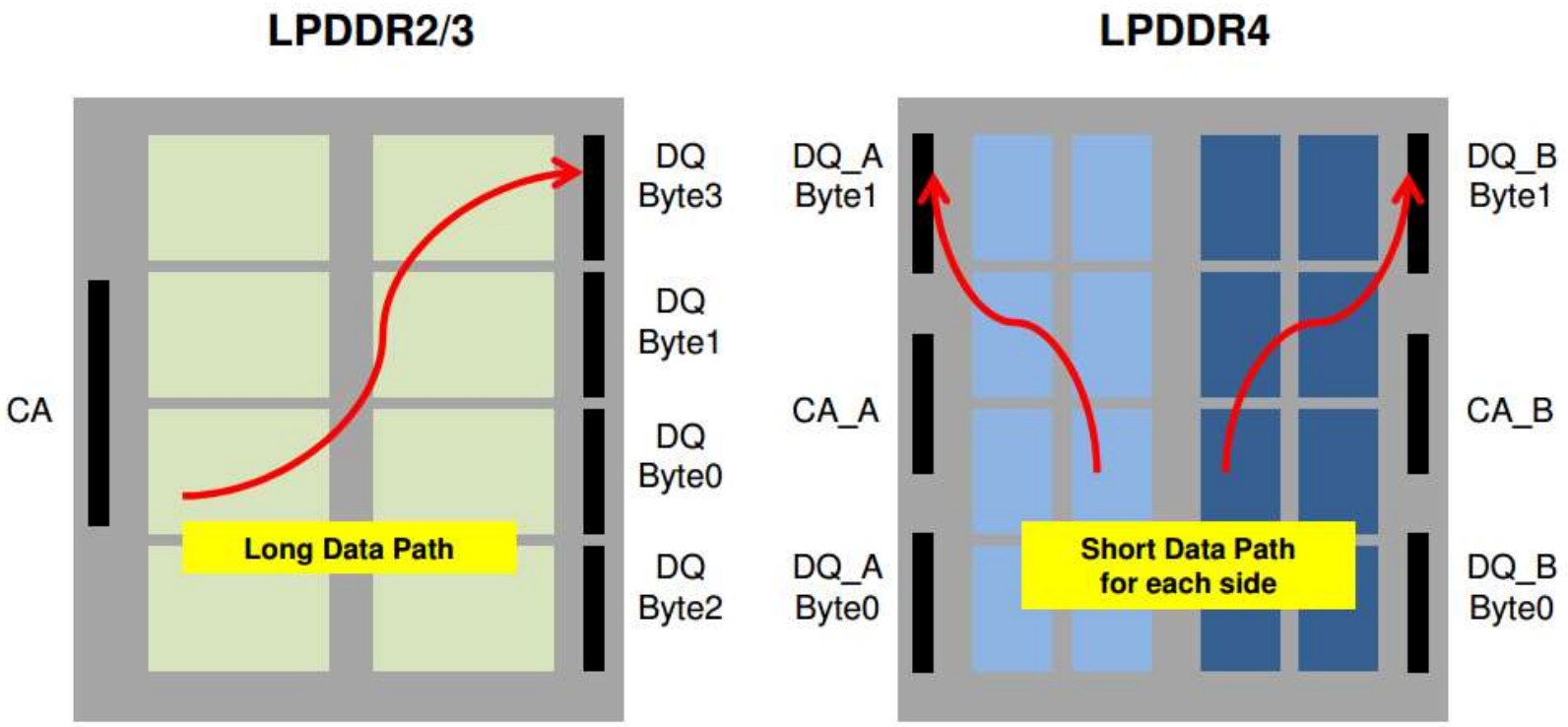


LPDDR4 Overview

	LPDDR3	LPDDR4	Notes
Channels	1 or 2	2	2 channels per die; LP4 channel = x16 Each LP4 channel has its own CA and Clock CA/Clock/DQ co-located on die
Clock Speed	400MHz to 1066MHz	800MHz to 2133MHz	Doubling the clock rate in LP4
Data Rate	800MT/s to 2133MT/s	1600MT/s to 4267MT/s	Doubling the data rate in LP4
Burst Length	8	16/32	Doubling Pre-fetch, core frequency is same
DQ ODT	No Termination, or 240/120 to VDDQ	VSSQ Termination	VSSQ = Ground
CA ODT	No Termination	VSSQ Termination	VSSQ = Ground
Vref	External	Internal	Vcent replaces Vref as reference for external measurements
Package	PoP/Discrete	PoP/Discrete	No change
I/O Voltage	1.2	1.1	Reduced Voltage
Preamble Postamble	Fixed	User selectable through MR	Makes it complicated to differentiate Read from Write
Voltage Swing	Close to rail/80%	~ 0.4 V	Reduced Swing
Read/Write Timing	Edge / Center Aligned	Edge/not Aligned	Writes need training for DQS to DQ relationship

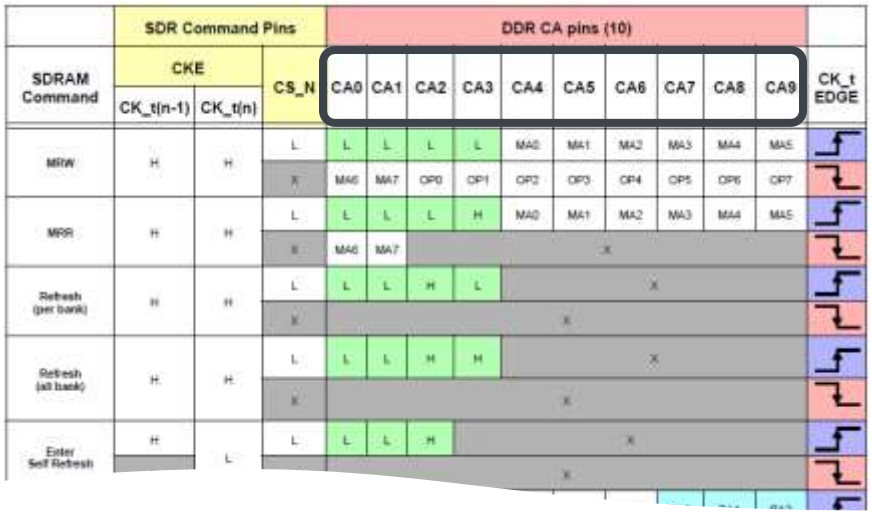
New Two Channel Dual Edge Pad Architecture

Reduced routing distance allows lower core power and high speed operation



New Command Definition for Lower Pin Count

- CA pins (per channel) reduced from 10 to 6
- LPDDR4 CA bus runs SDR
- Two and four-cycle command encoding



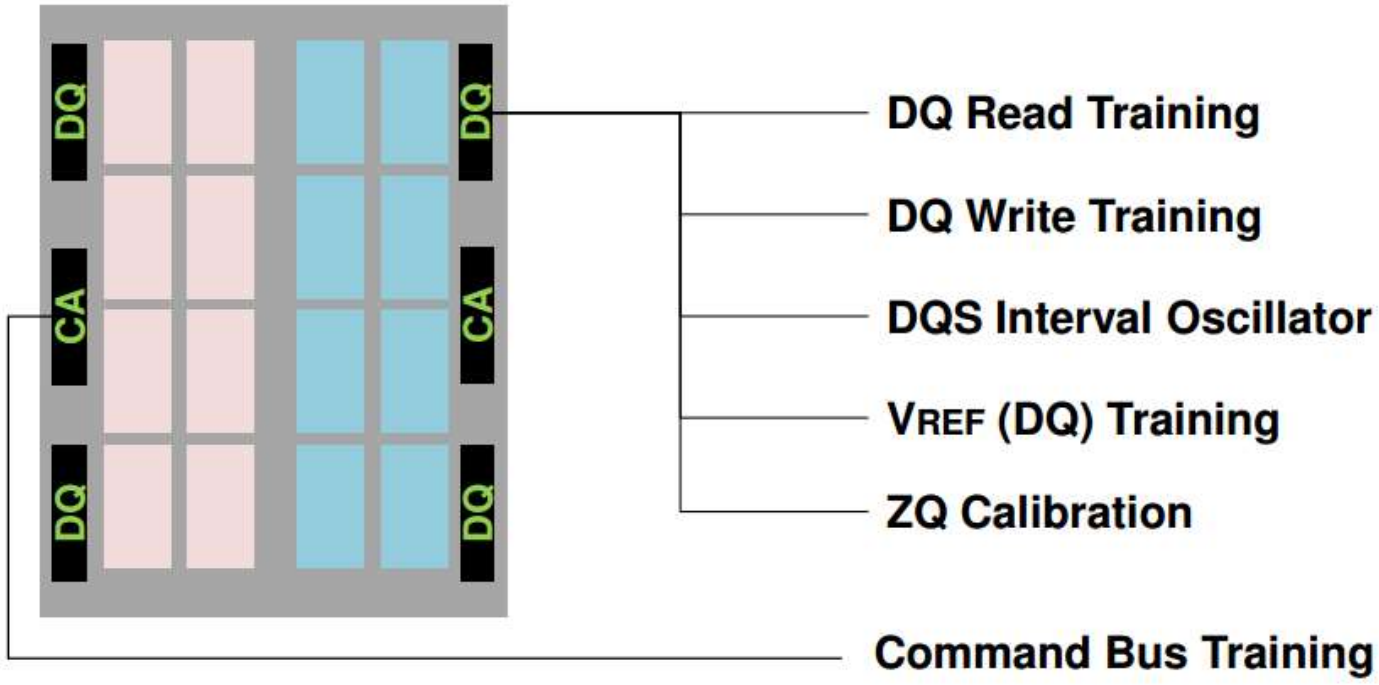
LPDDR2/3

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate -1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,2,3,10
	L	BA0	BA1	BA2	V	R10	R11	R2	
Activate -2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7, 9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write -2, Read-2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
		V						R2	
						H	V	R1	

LPDDR4

I/O Training / Calibration

To enable high speed operation, various training are needed.



- Two Frequency Set Points enable Rapid Frequency Switching
  - Stores calibration/training values at different frequencies
  - FSP settings can be saved and loaded via MR

CA Bus / DQ Bus Vcent

- LPDDR4 bus does not include (externally accessible) VREF.
- Vcent_CAx / Vcent_DQx is the Voltage at which the cumulative eye of the pin CAx / DQx is widest
- Vcent_CA(pin_mid) / Vcent_DQ(pin_mid) is defined as the middle between the largest and smallest Vcent_CA / Vcent_DQ within the group.
- Vcent_CA(pin_mid) / Vcent_DQ(pin_mid) is the best available estimate for the internal VREF (after training), that is accessible at the pins.

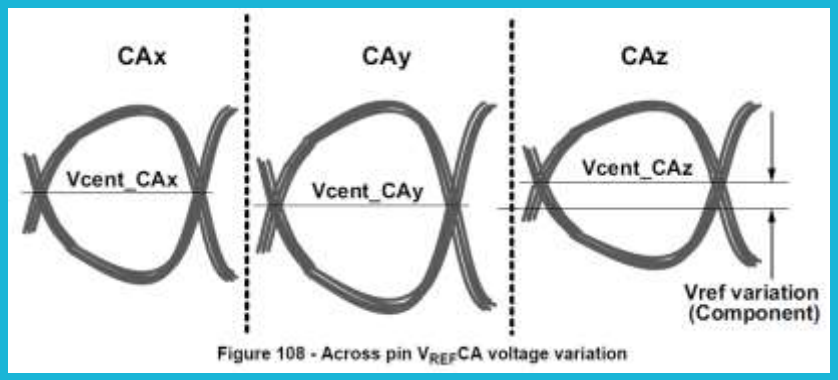


Figure 108 - Across pin V_{REF}CA voltage variation

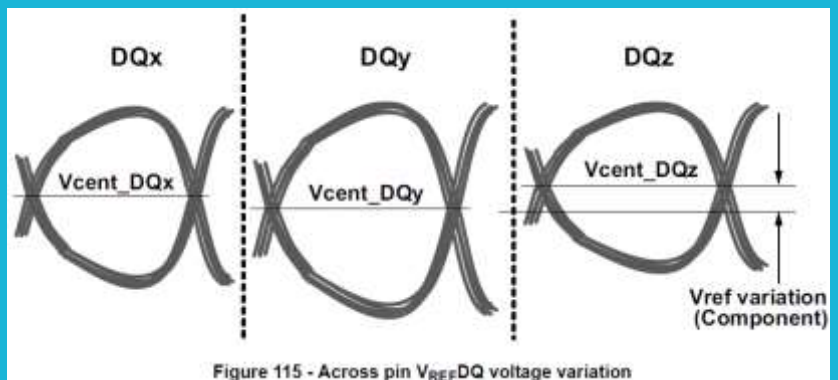


Figure 115 - Across pin V_{REF}DQ voltage variation

CA Bus / DQ Bus Mask-Based Timing and Voltage Definition

- All voltages are referenced to Vcent
- All timing referenced to rising clock edge / strobe edges
- Mask is centered around Vcent and rising clock edge / strobe edges

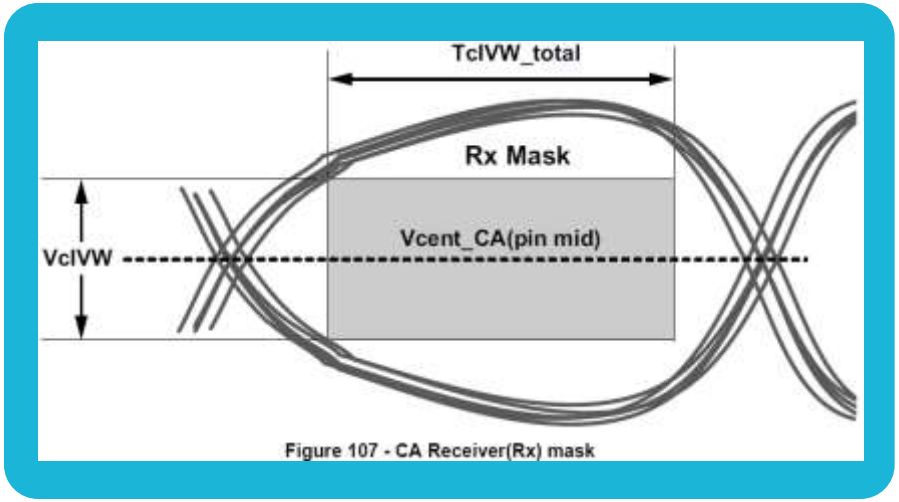


Figure 107 - CA Receiver(Rx) mask

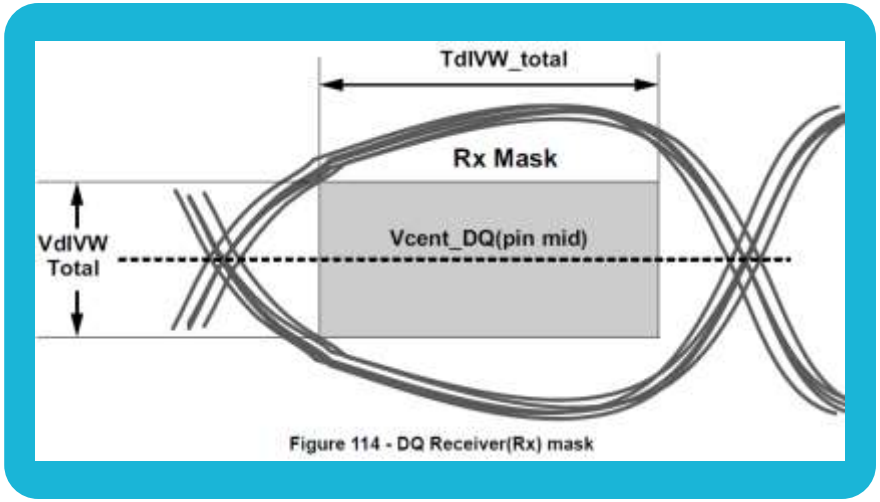


Figure 114 - DQ Receiver(Rx) mask

Conditions must be met cumulatively per group over time

CA Bus / DQ Bus

Minimum Voltage Level and Input Valid Window

- All voltages are referenced to Vcent

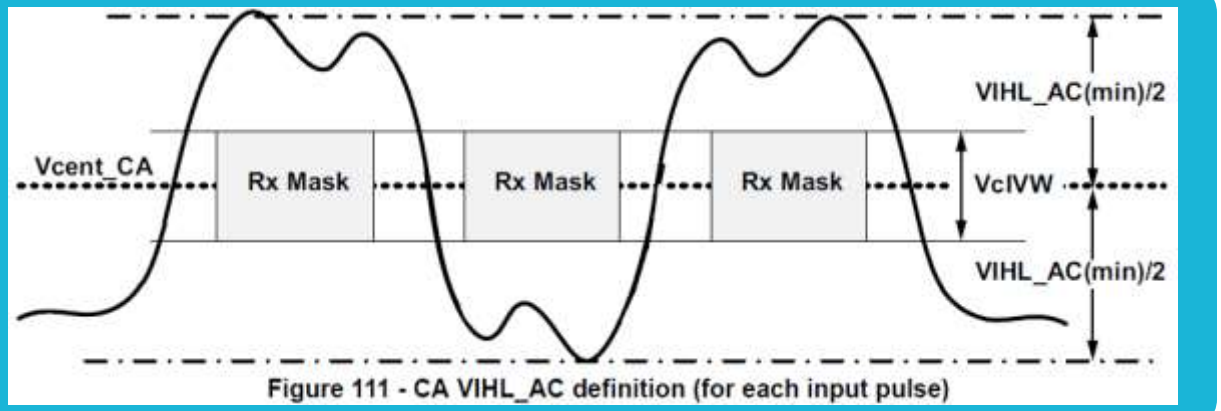


Figure 111 - CA VIHL_AC definition (for each input pulse)

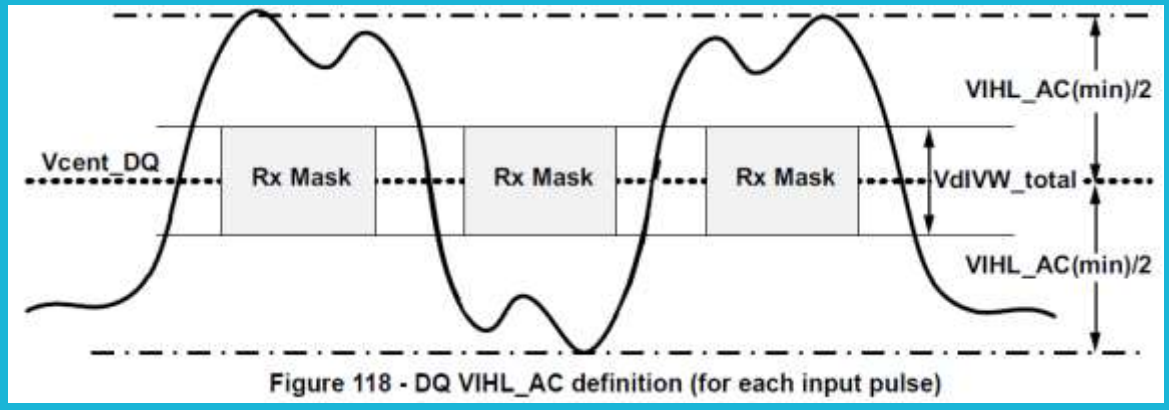


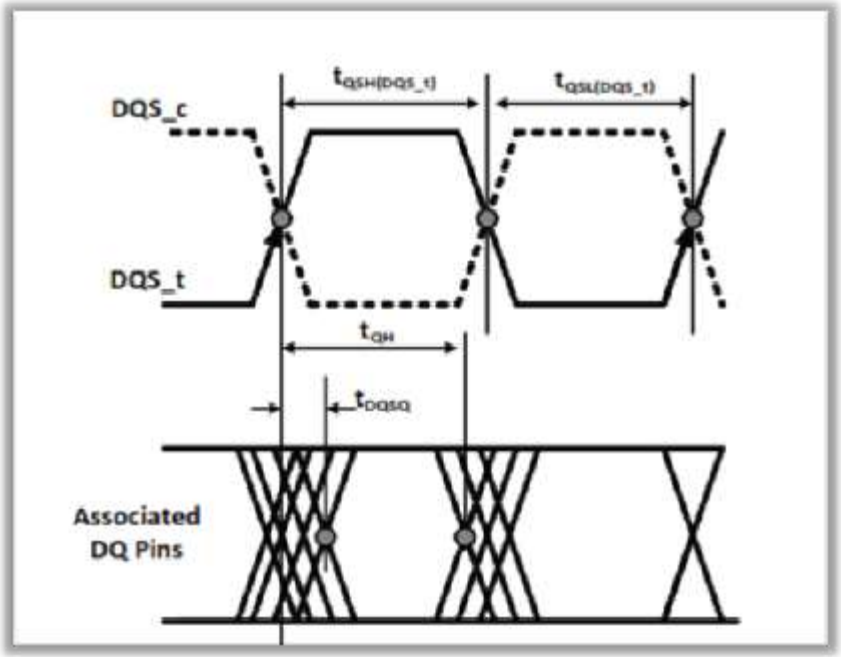
Figure 118 - DQ VIHL_AC definition (for each input pulse)

Conditions must be met for each individual UI

Read / Write Timing

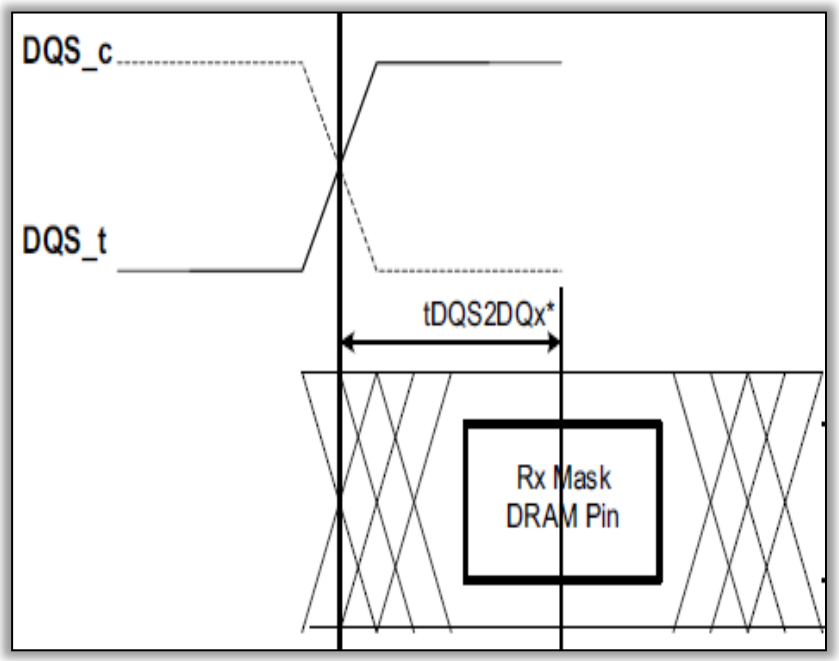
Read

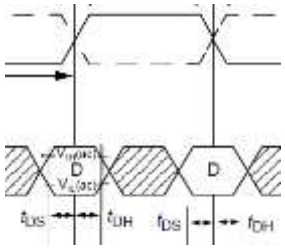
Data nominally EDGE aligned to strobe; similar to LPDDR2/3



Write

Data offset to strobe by tDQS2DQ; different from LPDDR2/3





For reference:
LPDDR2/3: center aligned

Voltage and Timing Numbers

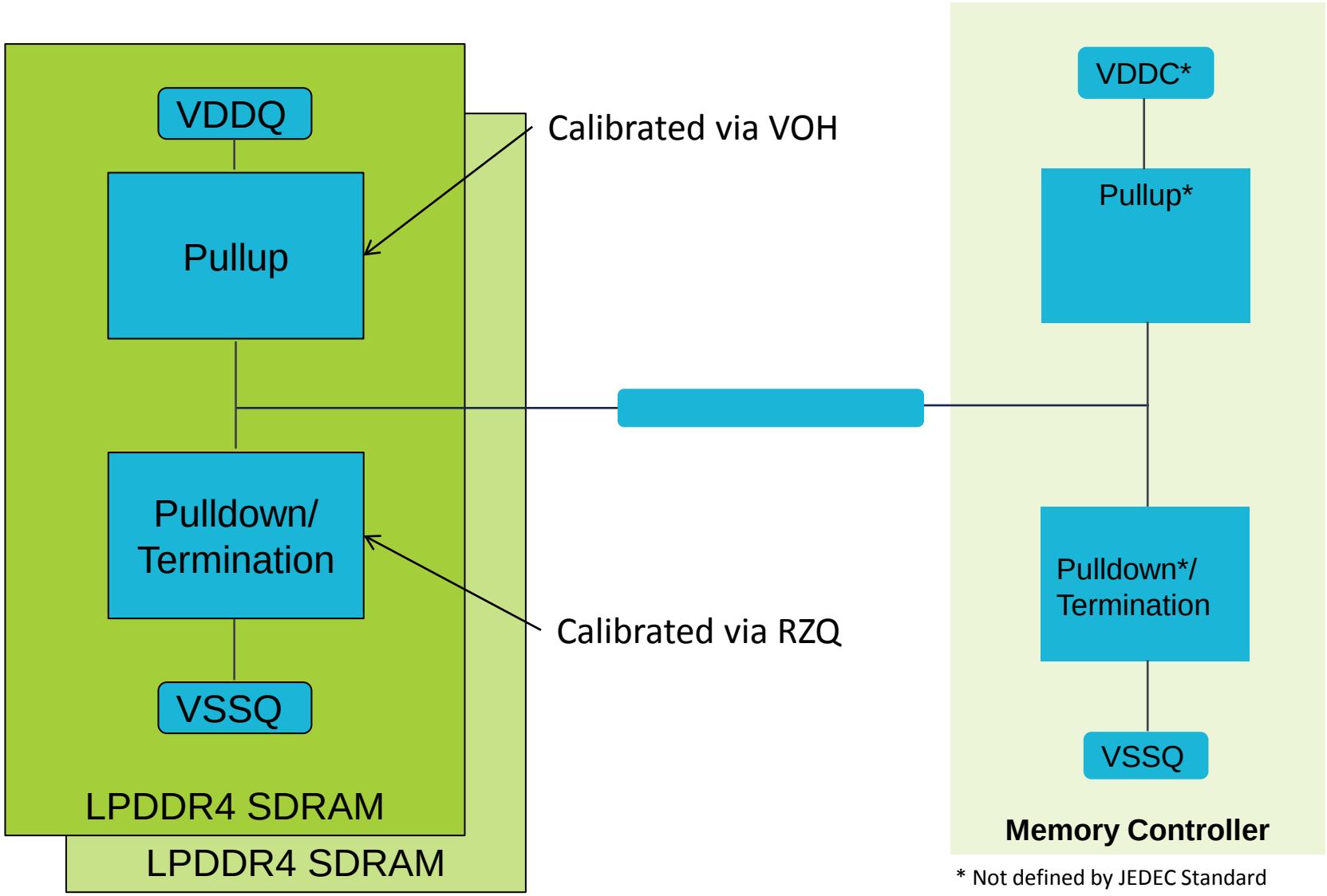
Data: DDR * UI=tCK(avg)min/2

Symbol	Parameter	1600/1867[A]		2133/2400		3200		4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	140	-	120	mV	1,2,3,5
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.22	-	0.22	-	0.25	-	0.25	UI*	1,2,4,5
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4, 5,14
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	170	-	mV	7,15
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		0.45		UI*	8
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	200	800	ps	9

CA: SDR * UI=tck(avg)min

Symbol	Parameter	DQ-1333[A]		DQ-1600/1867		DQ-3200		DQ-4266		Unit	NOTE
		min	max	min	max	min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	175	-	155	-	145	mV	1,2,4
TcIVW	Rx timing window	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3,4
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	190	-	180	-	mV	5,8
TcIPW	CA input pulse width	0.55		0.55		0.6		0.6		UI*	6

DQ Termination Scheme



* Not defined by JEDEC Standard

Beyond LPDDR4

- Low Voltage LPDDR4:
  - Same VDD1, VDD2
  - Reduced VDDQ = 0.6 V (for high speed terminated signaling) VOH ~ 0.5 · VDDQ
  - Reduced VDDQ = 0.4 V (for unterminated full swing at lower frequencies)
  - VDDQ changing dynamically

- LPDDR5 ….

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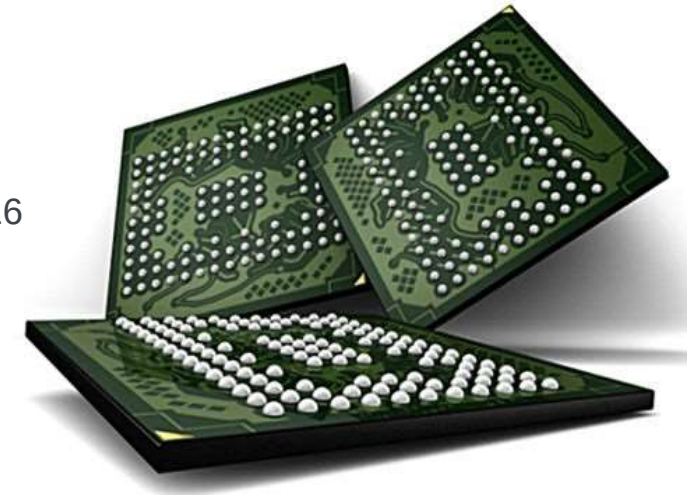
Signal Access for LPDDR Memory Technologies

3/14/2016

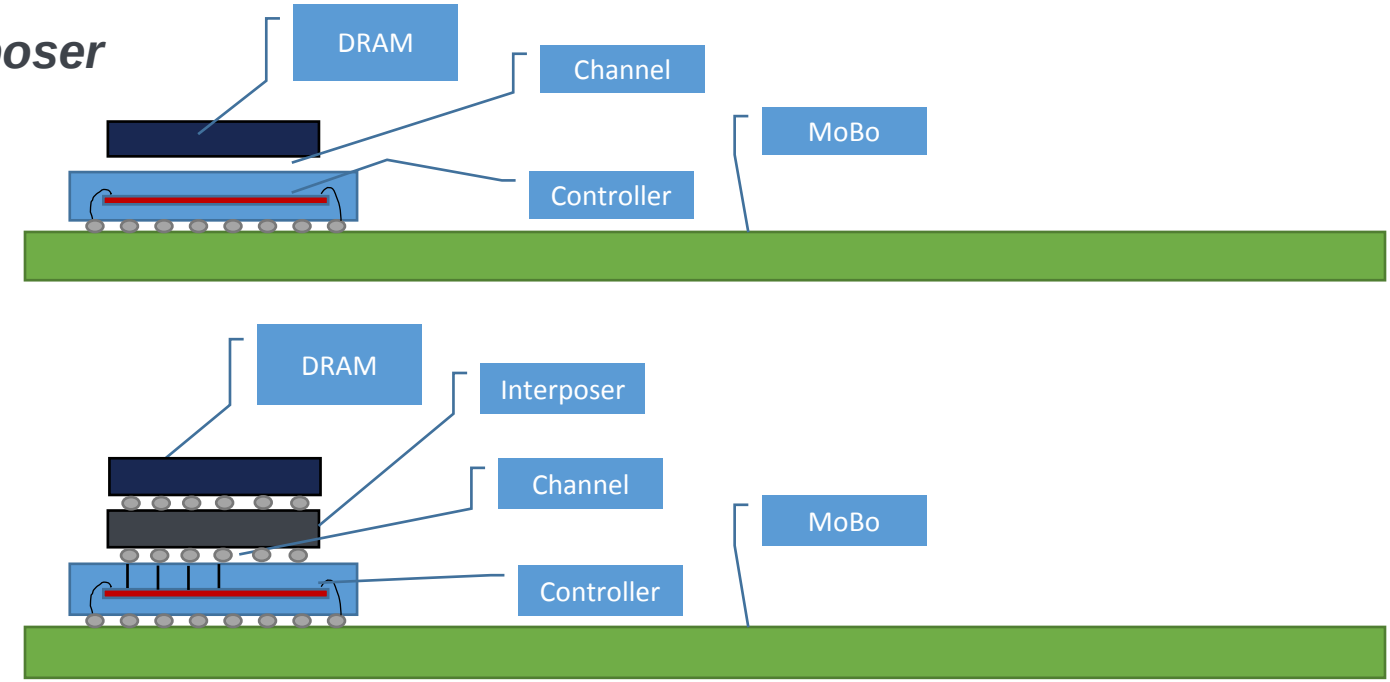


Section Agenda

- Interposer
  - Need
  - Interposer Port Naming
  - Modelling
  - Interposer Type
  - Interposer Availability
  - De-Embedding
  - Tri-Modes Probes

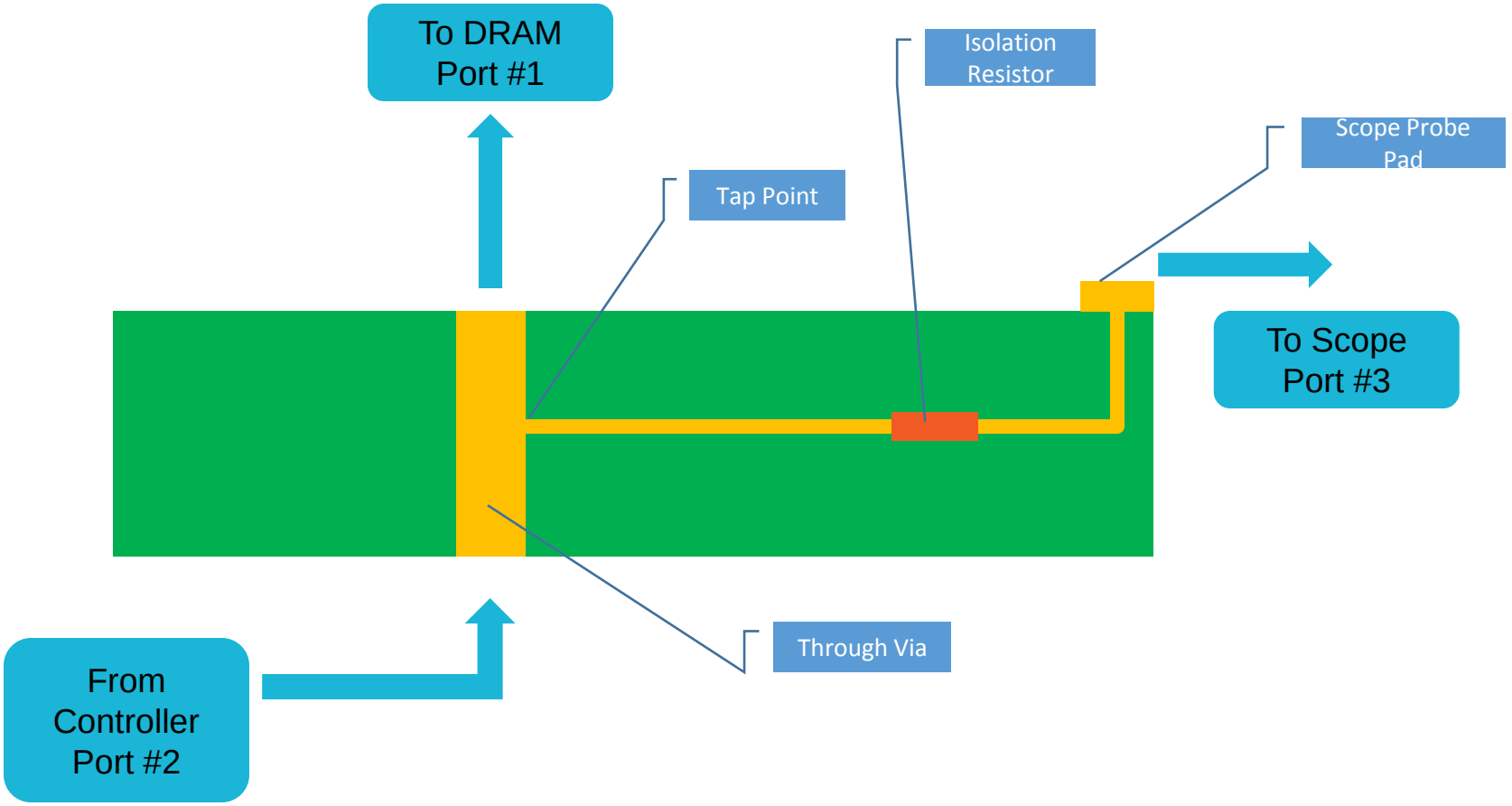
Probing

Interposer

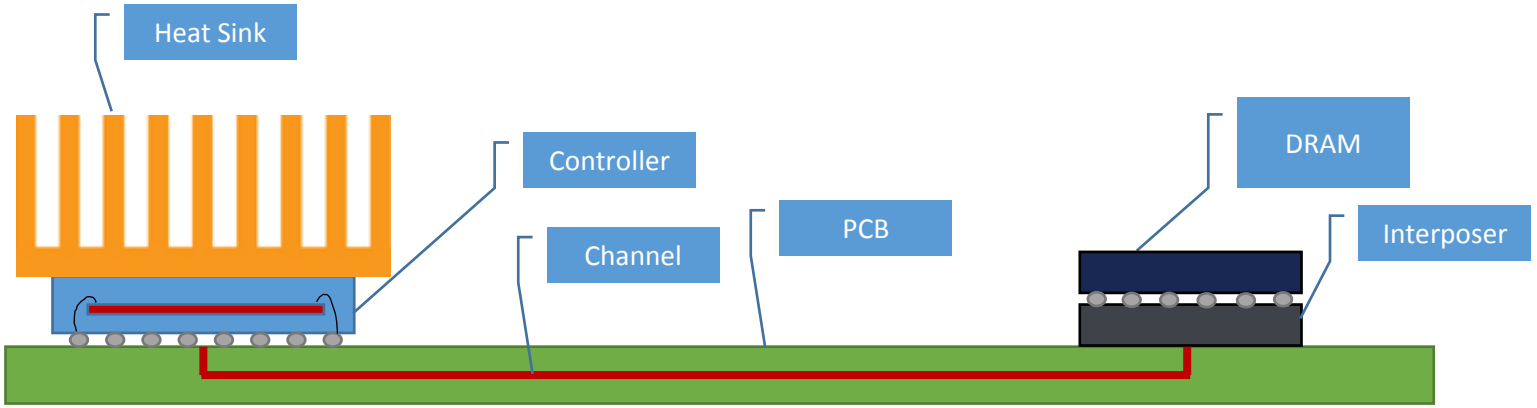


- An Interposer provides access to the signals for characterization and Debug
- Due to the density of the packages only a subset of all the signals are available for probing
- Custom probing solutions can be built if needed for specific applications

Interposer Port Naming



Modeling



- System level modeling is performed to study the signal behavior with probing solution in the channel path
- 2 port and 4 port S-parameter models that represent the probing system
- Two types of models represent the probing system
  - Loaded Models represent the case when the probe connected
  - Unloaded models represent the case when the probe is not connected

Interposer Types for Scope Probing

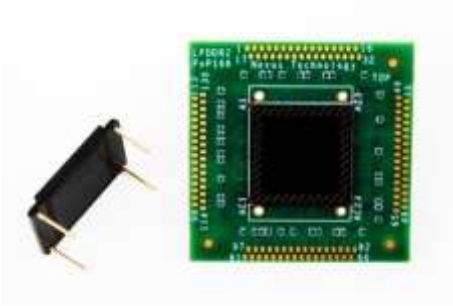
Socketed Interposers
- Large KoV (Keep out Volume)
- Easy to use with socket
- Access to more signals

Solder Down Interposers
- Larger KoV
- Access to more signals
- Low reusability

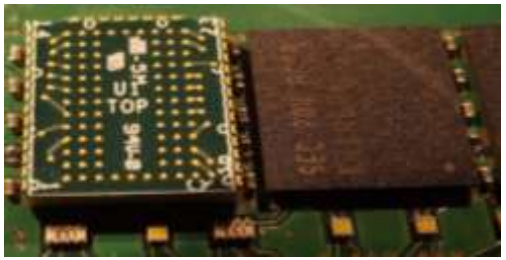
Edge Interposers
- Small KoV
- Access to less number of signals
- Low reusability

Custom Interposers
KoV as per design requirements
Mechanicals to match custom socketing
Signals as per specification

Solder Down interposer with Probe Pads



Socketed interposer for packages



Solder Down Interposer with Edge Style Probing

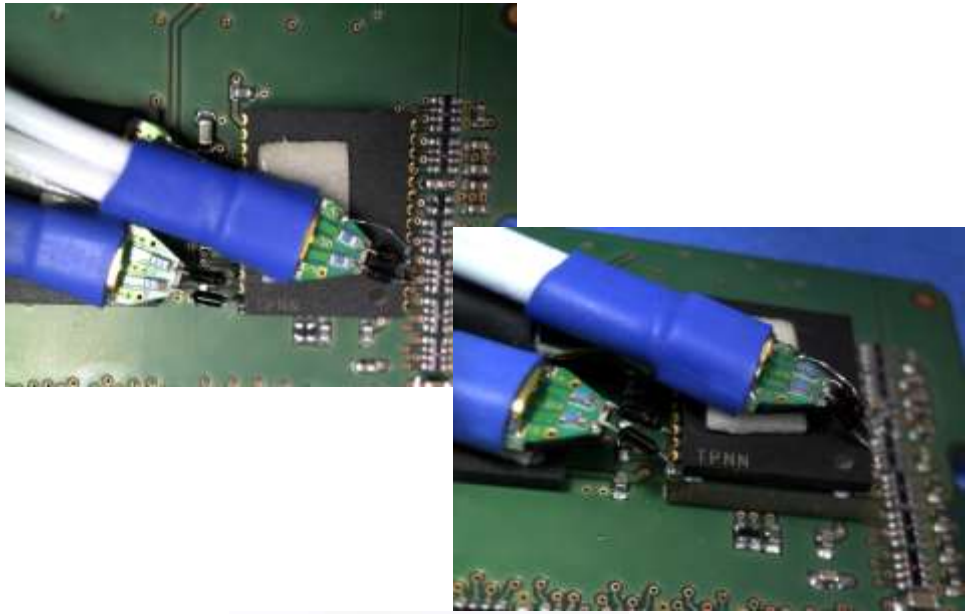
Socketed interposer with Probe Pads

Interposer Availability

Technology	Package / Form Factor
DDR2	Socketed – 60 Ball/ 84 Ball Solder-down – 60 Ball/ 84 Ball
DDR3	Socketed – 78 Ball/ 96 Ball Solder-down – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball – Coming soon! DIMM Interposer for MSO SO-DIMM Interposer for MSO
DDR4	Socketed – 78 Ball/ 96 Ball Edge Probe – 78 Ball/ 96 Ball Edge Probe – 144 Ball – Coming soon! DIMM Interposer for MSO
LPDDR	Socketed – 60ball
LPDDR2	Socketed – 136 ball/168 ball/216 ball/240 ball
LPDDR3	Socketed – 216 ball Solder-down – 178 ball
LPDDR4	Socketed – 272 ball Edge Probe – 272 ball Solder-down – 200 Ball Solder-down – 366 Ball
GDDR5	Socketed – 170 ball Solder – down – 170 ball

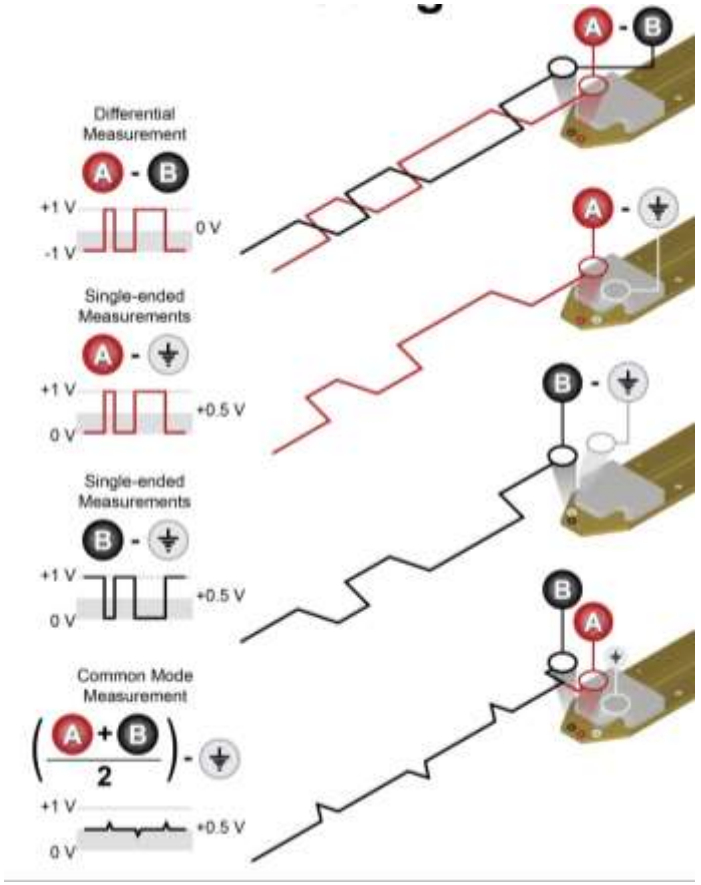
Probing LPDDR

- Requirements
  - Multiple connections
  - Tight spaces
  - High performance
  - Solder-in connectivity
- Performance Probes
  - Consist of scope connection, >1m length cable, amplifier and attenuation stages
  - Accessory tips



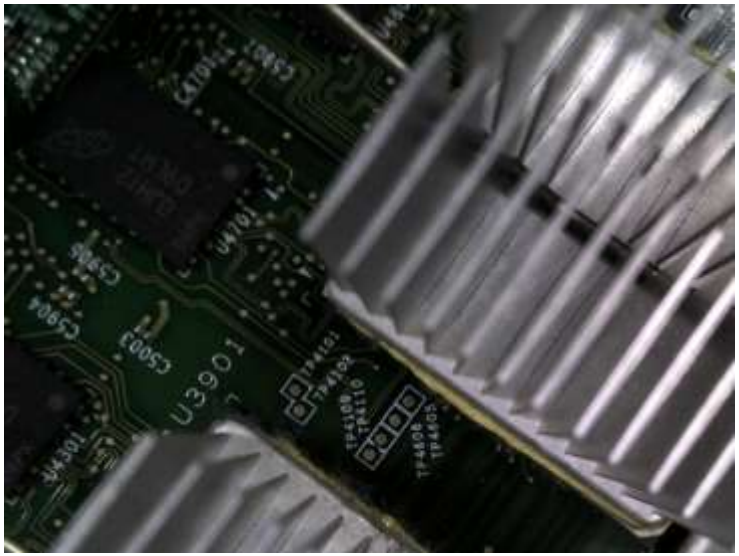
TriMode™ Probes

- TriMode, with a single probe-DUT connection, allows:
  - Traditional differential measurements
  - Independent single ended measurements on either input
    - V+ with respect to ground
    - V- with respect to ground
  - Direct common mode measurements
- Another use of TriMode
  - Connecting 2 single ended signals, such as DQ0 and DQ0
  - Switching between the data signals via the scope's UI for a measurement on each DQ

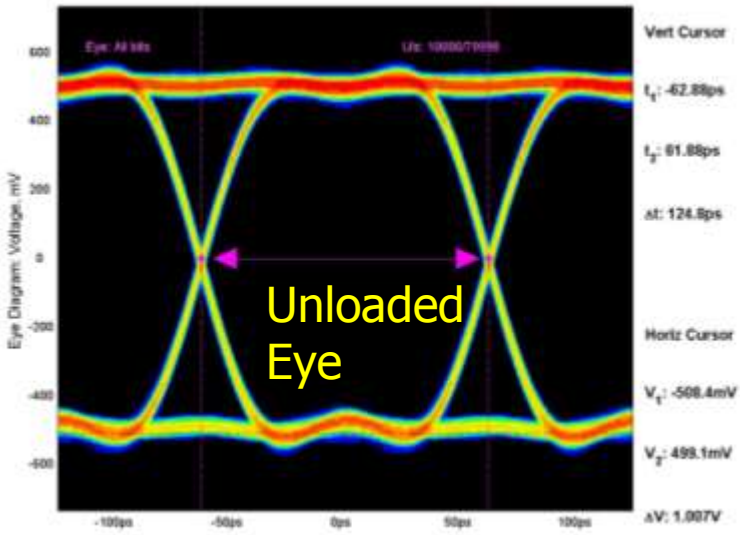


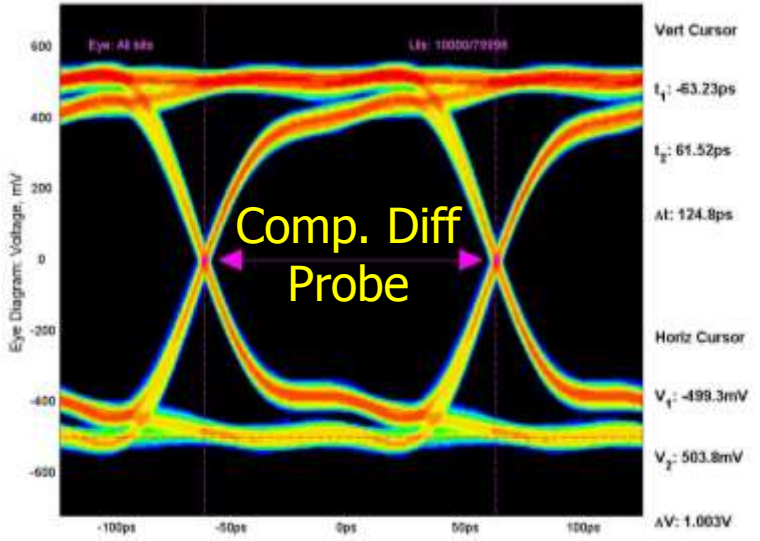
Other Signal Access Challenges

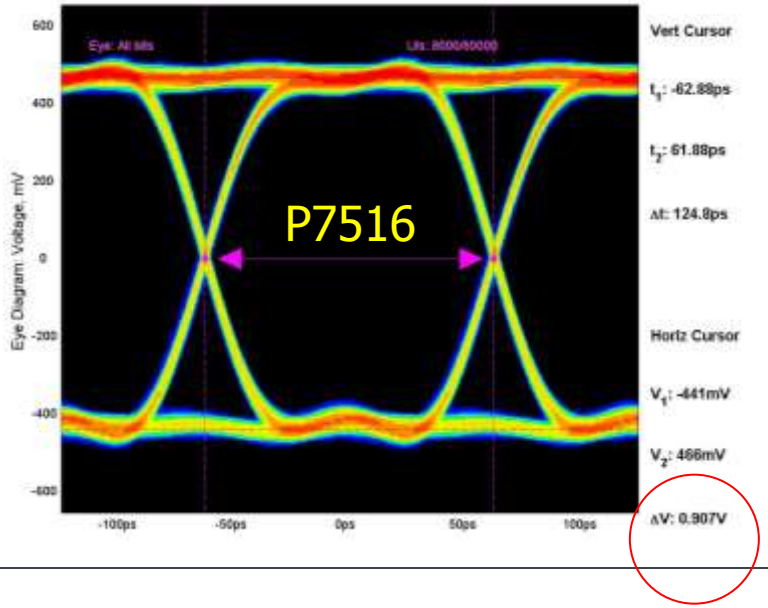
- Connections between DIMM slots
- Connections inside of a closed chassis
- Crowded boards with large components blocking access to the test points



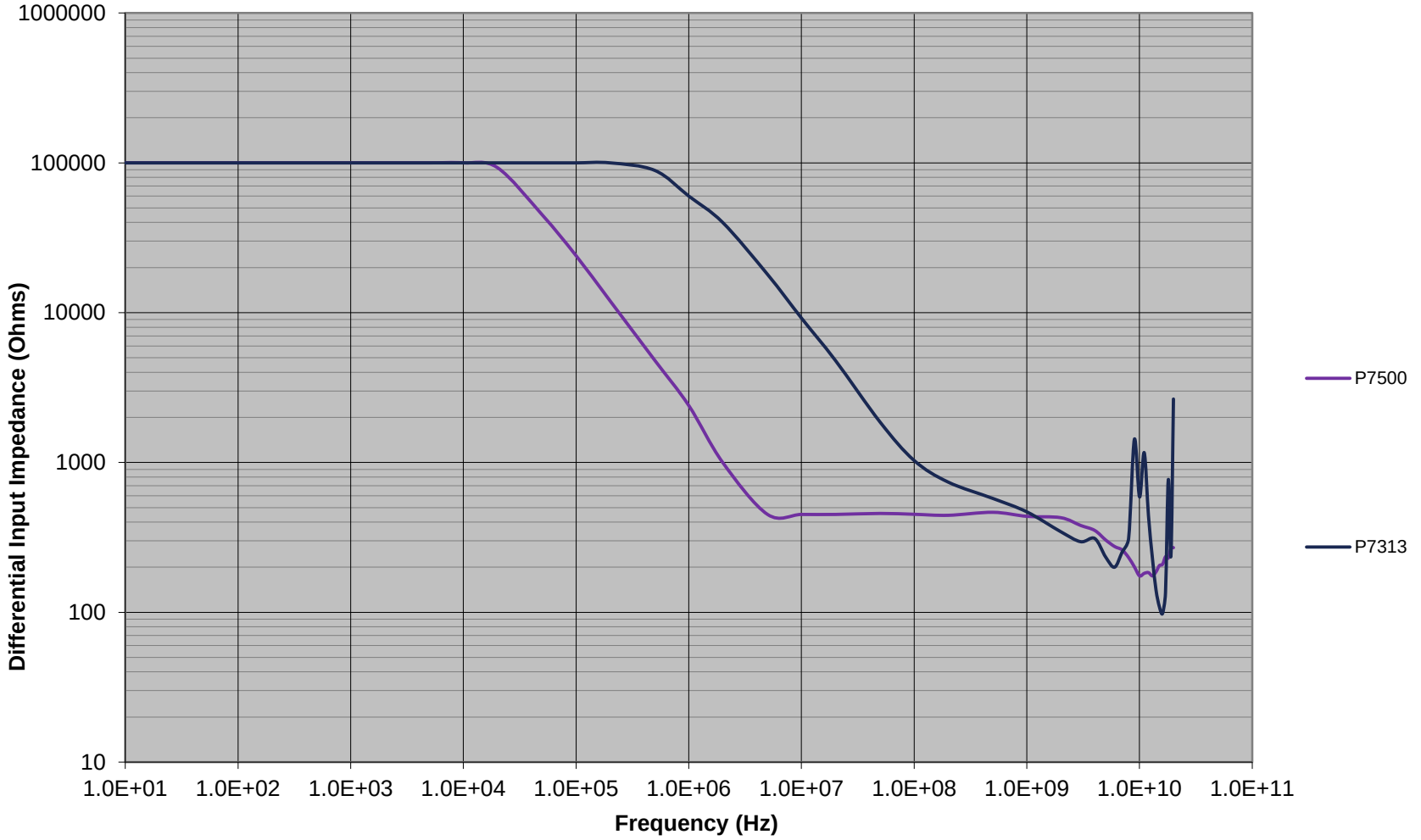
Impact of attaching a probe 8Gb/s Eye



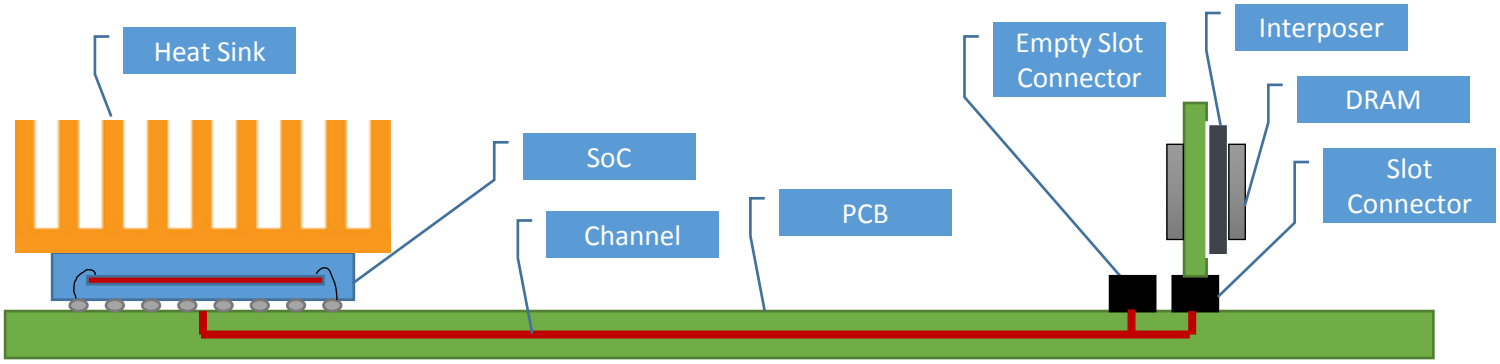




Performance Probe Differential Input Impedance



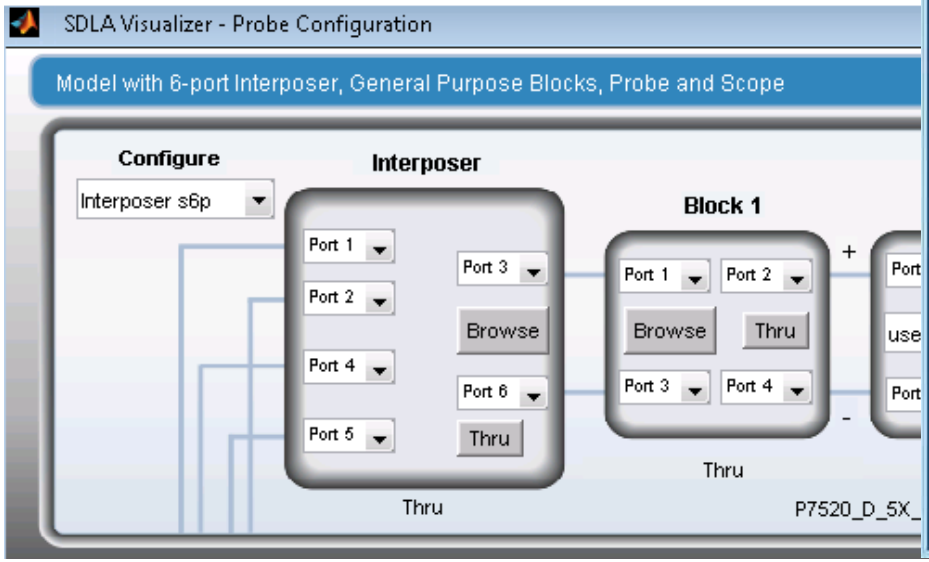
De-embedding / Virtual Probing

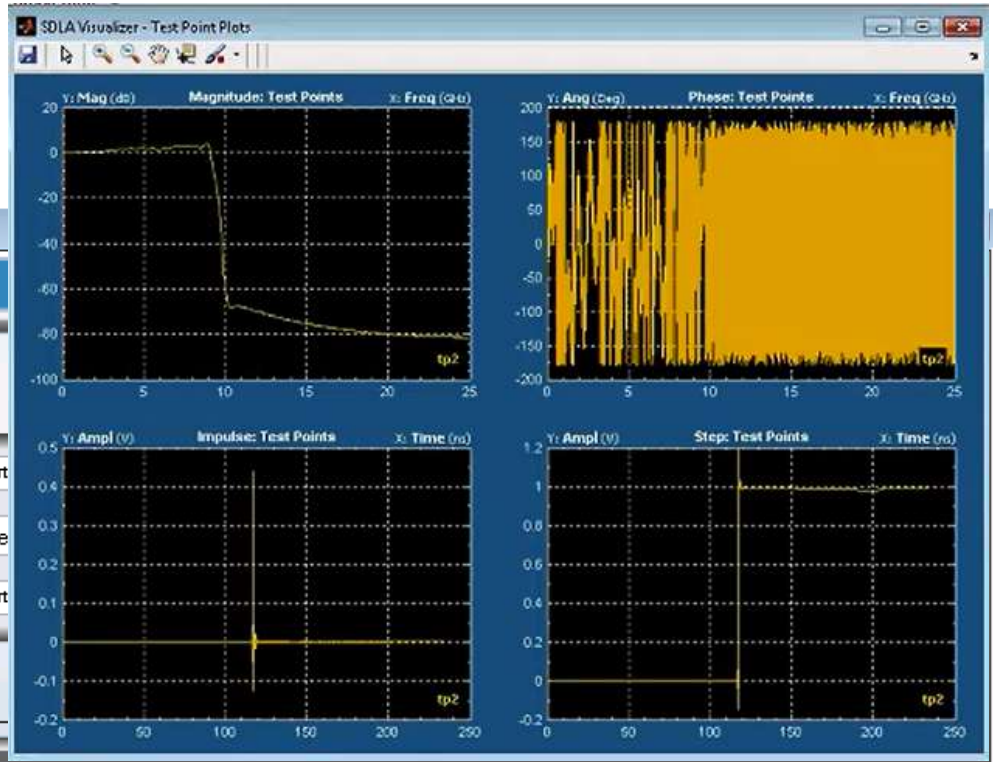


- In order to remove the effects of the Interposer/Probe, De-embedding must be considered.
- S-Parameters of the objects that need to be de-embedded are required for de-embedding
- S-Parameters for the Interposer will be made available and can be used to create De-embed filters.
- S-parameters can be extracted
  - From the 3D models by simulation
  - Measuring on a real sample using a VNA or TDR method on sampling scope

De-embed Filter

- Model the probing setup Use the S-Parameter Models to generate Filters
- Supports different blocks in the signal path including
  - Interposer
  - Probe / tip
  - RF Switch





P7700 High Bandwidth TriMode™ Probe is coming……

NEW! Active input directly at the probe tip

NEW! TekFlex™ accessories

- Improved access to tight test locations

Best-in-Class low loading for LPDDR and MIPI standard

Industry's lowest cost per connection

Tektronix

Thank You!

3/14/2016